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File 348:EUROPEAN PATENTS 1978-2006/ 200624

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File 349:PCT FULLTEXT 1979-2006/UB=20060615,UT=20060608

(c) 2006 WIPO/Univentio

File 350:Derwent WPIX 1963-2006/UD,UM &UP=200639

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Set	Items	Description
S1	15	(PROCESS???(2W)BLOCK? ?)(50N)(VIRTUALI?AT?)

1/3,K/1 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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01378612 **Image available**

A RUNTIME ADAPTABLE SECURITY PROCESSOR

PROCESSEUR DE SURETE MODIFIABLE EN FONCTIONNEMENT

Patent Applicant/Inventor:

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Legal Representative:

LEAL Peter R (agent), DLA Piper Rudnick Gray Cary US LLP, 2000 University
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Patent and Priority Information (Country, Number, Date):

Patent: WO 200660571 A2 20060608 (WO 0660571)

Application: WO 2005US43469 20051202 (PCT/WO US2005043469)

Priority Application: US 20044742 20041202

Designated States:

(All protection types applied unless otherwise stated - for applications
2004+)

AE AG AL AM AT AU AZ BA BB BG BR BW BY BZ CA CH CN CO CR CU CZ DE DK DM
DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KM KN KP KR
KZ LC LK LR LS LT LU LV LY MA MD MG MK MN MW MX MZ NA NG NI NO NZ OM PG
PH PL PT RO RU SC SD SE SG SK SL SM SY TJ TM TN TR TT TZ UA UG US UZ VC
VN YU ZA ZM ZW

(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LT LU LV MC NL
PL PT RO SE SI SK TR

(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG

(AP) BW GH GM KE LS MW MZ NA SD SL SZ TZ UG ZM ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English

Filing Language: English

Fulltext Word Count: 46697

Fulltext Availability:

Detailed Description

Detailed Description

... a high performance routing engine, a high performance network
management engine, deep packet inspection engine providing string search,
an engine for XML, an engine for **virtualization**, and the like,
providing support for an application specific acceleration. The
processing capability of this IP processor can be scaled by scaling the
number of SAN Packet **Processor blocks** 1706 (a) through 1706 (n) in
the chip to meet the line rate requirements of the network interface. The
I 0 primary limitation from the...

1/3,K/2 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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01377363

PREVENTION OF DATA LOSS DUE TO POWER FAILURE

PREVENTION DES PERTES DE DONNEES DUES A UNE PANNE DE COURANT

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Legal Representative:

VINCENT Lester J et al (agent), Blakely Sokoloff Taylor & Zafman, 12400
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Patent and Priority Information (Country, Number, Date):

Patent: WO 200660237 A2 20060608 (WO 0660237)

Application: WO 2005US42314 20051117 (PCT/WO US2005042314)

Priority Application: US 20044710 20041203

Designated States:

(All protection types applied unless otherwise stated - for applications
2004+)

AE AG AL AM AT AU AZ BA BB BG BR BW BY BZ CA CH CN CO CR CU CZ DE DK DM
DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KM KN KP KR
KZ LC LK LR LS LT LU LV LY MA MD MG MK MN MW MX MZ NA NG NI NO NZ OM PG
PH PL PT RO RU SC SD SE SG SK SL SM SY TJ TM TN TR TT TZ UA UG US UZ VC
VN YU ZA ZM ZW

(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LT LU LV MC NL
PL PT RO SE SI SK TR

(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG

(AP) BW GH GM KE LS MW MZ NA SD SL SZ TZ UG ZM ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English

Filing Language: English

Fulltext Word Count: 6851

Fulltext Availability:

Detailed Description

Detailed Description

... process will be described using the computing system 300 as shown in
Figure 3, although this example process applies to any other computing
systems. The **process** starts with **block** 405 where an AC power failure
occurs. Assume that a hardware **virtualization** environment runs on the
computing system, states of hardware components in the computing system
300 just before the AC power failure occurs may be stored...

1/3,K/3 (Item 3 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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01343072 **Image available**

PERSONALIZED HEADPHONE VIRTUALIZATION

VIRTUALISATION D'ECOUTEURS PERSONNALISEE

Patent Applicant/Assignee:

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GB

Patent and Priority Information (Country, Number, Date):

Patent: WO 200624850 A2-A3 20060309 (WO 0624850)

Application: WO 2005GB3372 20050901 (PCT/WO GB2005003372)

Priority Application: GB 2004193462 20040901

Designated States:

(All protection types applied unless otherwise stated - for applications
2004+)

AE AG AL AM AT AU AZ BA BB BG BR BW BY BZ CA CH CN CO CR CU CZ DE DK DM
DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KM KP KR KZ
LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NA NG NI NO NZ OM PG PH PL
PT RO RU SC SD SE SG SK SL SM SY TJ TM TN TR TT TZ UA UG US UZ VC VN YU
ZA ZM ZW

(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LT LU LV MC NL
PL PT RO SE SI SK TR

(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG

(AP) BW GH GM KE LS MW MZ NA SD SL SZ TZ UG ZM ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English

Filing Language: English

Fulltext Word Count: 36406

Fulltext Availability:

Detailed Description

Detailed Description

... intended head orientation scope.

[00621 FIG. 3 5 illustrates a plan view of human subject undergoing a
headphone equalization measurement and the connections to related
processing blocks .

[00631 FIG. 36 illustrates the **virtualization** process for a single
channel using sub-band convolution where the inter-aural time delays are
implemented in the time-band domain following the synthesis filter bank.

8 [00641 FIG. 37 illustrates the **virtualization** process for a single
channel using sub-band convolution where the inter-aural time delays are
implemented in the sub-band domain prior to the...

1/3,K/4 (Item 4 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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01306786 **Image available**

RUNTIME ADAPTABLE PROTOCOL PROCESSOR

PROCESSEUR DE PROTOCOLE ADAPTABLE EN COURS D'EXECUTION

Patent Applicant/Inventor:

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Patent and Priority Information (Country, Number, Date):

Patent: WO 2005114339 A2 20051201 (WO 05114339)

Application: WO 2005US16352 20050509 (PCT/WO US05016352)

Priority Application: US 2004845345 20040512

Designated States:

(All protection types applied unless otherwise stated - for applications
2004+)

AE AG AL AM AT AU AZ BA BB BG BR BW BY BZ CA CH CN CO CR CU CZ DE DK DM
DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KM KP KR KZ
LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NA NG NI NO NZ OM PG PH PL
PT RO RU SC SD SE SG SK SL SM SY TJ TM TN TR TT TZ UA UG US UZ VC VN YU
ZA ZM ZW

(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LT LU MC NL PL
PT RO SE SI SK TR

(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG

(AP) BW GH GM KE LS MW MZ NA SD SL SZ TZ UG ZM ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English

Filing Language: English

Fulltext Word Count: 38184

Fulltext Availability:

Detailed Description

Detailed Description

... a high performance routing engine, a high performance network
management engine, deep packet inspection engine providing string search,
an engine for XIVIL, an engine for **virtualization**, and the like,
providing support for an application specific acceleration. The
processing capability of this IP processor can be scaled by scaling the
number of SAN Packet **Processor blocks** 1706 (a) through 1706 (n) in
the chip to meet the line rate requirements of the network interface. The
primary limitation from the scalability would...

1/3,K/5 (Item 5 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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01291997

**PROVIDING SUPPORT FOR SINGLE STEPPING A VIRTUAL MACHINE IN A VIRTUAL
MACHINE ENVIRONMENT**

**AIDE A L'EXECUTION PAS A PAS D'UNE MACHINE VIRTUELLE DANS UN ENVIRONNEMENT
DE MACHINE VIRTUELLE**

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Patent and Priority Information (Country, Number, Date):

Patent: WO 200598616 A2 20051020 (WO 0598616)
Application: WO 2005US10156 20050325 (PCT/WO US05010156)
Priority Application: US 2004814569 20040330

Designated States:

(All protection types applied unless otherwise stated - for applications
2004+)

AE AG AL AM AT AU AZ BA BB BG BR BW BY BZ CA CH CN CO CR CU CZ DE DK DM
DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC
LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NA NI NO NZ OM PG PH PL PT RO
RU SC SD SE SG SK SL SM SY TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM
ZW

(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LT LU MC NL PL
PT RO SE SI SK TR

(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG

(AP) BW GH GM KE LS MW MZ NA SD SL SZ TZ UG ZM ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English

Filing Language: English

Fulltext Word Count: 8694

Fulltext Availability:

Detailed Description

Detailed Description

... not the other data) or correctness (e.g., the data may need to be

changed prior to writing it to the device if required by **virtualization**).

[00651 If the decision made at decision box 518 is positive, processing logic in the VNM writes the data to the device (**processing block** 520). Alternatively, the VMM may modify the data before writing it to the device to ensure that certain characteristics regarding, for example, security, performance or device **virtualization** are proper. [00661 Thus, a method and apparatus for providing support for single stepping a virtual machine in a virtual machine environment have been described...

1/3,K/6 (Item 6 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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01288508 **Image available**

INTERFACE FOR DISTRIBUTED PROCESING OF SCSI TASKS

INTERFACE DE TRAITEMENT DISTRIBUE DES TACHES SCSI

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Patent and Priority Information (Country, Number, Date):

Patent: WO 200594209 A2-A3 20051013 (WO 0594209)

Application: WO 2004US24695 20040731 (PCT/WO US04024695)

Priority Application: US 2004794694 20040305

Designated States:

(All protection types applied unless otherwise stated - for applications
2004+)

AE AG AL AM AT AU AZ BA BB BG BR BW BY BZ CA CH CN CO CR CU CZ DE DK DM
DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC
LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NA NI NO NZ OM PG PH PL PT RO
RU SC SD SE SG SK SL SY TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PL PT RO
SE SI SK TR

(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG

(AP) BW GH GM KE LS MW MZ NA SD SL SZ TZ UG ZM ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English

Filing Language: English

Fulltext Word Count: 18378

Fulltext Availability:

Detailed Description

Detailed Description

... command, just to list a few. Storage management devices have been designed to process SCSI tasks and perform storage operations, such as RAID or storage **virtualization** and then deliver commands to physical devices. A Front End Transport (FET) receives SCSI commands using a transport specific protocol. A Back End Transport (BET) issues SCSI commands using the same or different transport specific protocol. A **processing block** processes tasks presented via one or more FETs and issues tasks to one or more BETs. There is no relationship as to the number of...

...Accordingly, the interface 20 remains independent of whether the transport is iSCSI, FCP, and so forth.

SCSI tasks requiring processing are routed to a SCSI **processing block** 34. The operations required for processing SCSI tasks are well known in the art. In addition, **processing blocks** 36 perform storage application functions such as RAID or storage **virtualization**. After any necessary processing, one or more mapped I/O are passed to a BET 38 where the command is sent out across a SAN...

1/3,K/7 (Item 7 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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01276022 **Image available**

**A DISTRIBUTED NETWORK SECURITY SYSTEM AND HARDWARE PROCESSOR THEREFOR
SYSTEME DE SECURITE A RESEAU DISTRIBUE ET MATERIEL DE TRAITEMENT
CORRESPONDANT**

Patent Applicant/Inventor:

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Legal Representative:

LEAL Peter R (agent), DLA Piper Rudnick Gray Cary US LLP, Attn: Patent
Department, 2000 University Avenue, East Palo Alto, CA 94303-2248, US,
Patent and Priority Information (Country, Number, Date):

Patent: WO 200581855 A2-A3 20050909 (WO 0581855)

Application: WO 2005US5159 20050218 (PCT/WO US05005159)

Priority Application: US 2004783890 20040220

Designated States:

(All protection types applied unless otherwise stated - for applications
2004+)

AE AG AL AM AT AU AZ BA BB BG BR BW BY BZ CA CH CN CO CR CU CZ DE DK DM
DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC
LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NA NI NO NZ OM PG PH PL PT RO
RU SC SD SE SG SK SL SM SY TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM
ZW

(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LT LU MC NL PL
PT RO SE SI SK TR

(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG

(AP) BW GH GM KE LS MW MZ NA SD SL SZ TZ UG ZM ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English

Filing Language: English

Fulltext Word Count: 30968

Fulltext Availability:

Detailed Description

Detailed Description

... a high performance routing engine, a high performance network
management engine, deep packet inspection engine providing string search,
an engine for XMIL, an engine for **virtualization**, and the like,
providing support for an application specific acceleration. The
processing capability of this IP processor can be scaled by scaling the
number of SAN Packet **Processor blocks** 1706 (a) through 1706 (n) in
the chip to meet the line rate requirements of the network interface. The
primary limitation from the scalability would...

1/3,K/8 (Item 8 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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01173736

A METHOD FOR CPU SIMULATION USING VIRTUAL MACHINE EXTENSIONS
PROCEDE DE SIMULATION D'UNITE CENTRALE FAISANT APPEL A DES EXTENSIONS DE
MACHINE VIRTUELLE

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Patent and Priority Information (Country, Number, Date):

Patent: WO 200495283 A2-A3 20041104 (WO 0495283)

Application: WO 2004US4092 20040211 (PCT/WO US04004092)

Priority Application: US 2003395557 20030324

Designated States:

(All protection types applied unless otherwise stated - for applications
2004+)

AE AG AL AM AT AU AZ BA BB BG BR BW BY BZ CA CH CN CO CR CU CZ DE DK DM
DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC
LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NA NI NO NZ OM PG PH PL PT RO
RU SC SD SE SG SK SL SY TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT RO SE
SI SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) BW GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English

Filing Language: English

Fulltext Word Count: 2820

Fulltext Availability:

Detailed Description

Detailed Description

... process on top of the Host OS.

Figure 3 is a flow diagram of one embodiment of the operation of Full
Platform Simulator 222. At **processing** block 310, simulation begins. At
decision block 320, Platform Simulator 222 determines whether to switch
to Direct Execution.

[0028] If Platform Simulator 222 decides to switch to Direct Execution,
Monitor 224 is invoked with request to launch (or resume) Direct
Execution and a guest state is virtualized, **processing** block 330.
Otherwise, simulation continues at Platform Simulator 222, **processing**
block 380. At **processing** block 340, the Virtual Machine is launched
(or resumed). Subsequently, the Virtual Machine begins to run guest OS
code.

[00291 At some time during the running of the guest OS code, a sensitive
(or virtualization) event occurs. Therefore, at **processing** block 350,
the Virtual Machine is exited and the current state is saved/restored. At

decision block 360', it is determined whether the sensitive event is a complex event. If the event is not a complex event, the event is a virtualization event, and the virtualization event is managed at **processing block 365**. Subsequently, control is returned to **processing block 330** where the guest state is virtualized.

[00301 If the event is a complex event, the guest state is de-virtualized, **processing block 370**. At **processing block 380**, instructions are again simulated. At decision block 390, it is determined whether the simulation has ended. If not, control is returned to processing block...

1/3,K/9 (Item 9 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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01075431 **Image available**

HIGH PERFORMANCE IP PROCESSOR FOR TCP/IP, RDMA AND IP STORAGE APPLICATIONS
PROCESSEUR IP A PERFORMANCE ELEVEE POUR DES APPLICATIONS DE STOCKAGE
TCP/IP, RDMA ET IP

Patent Applicant/Inventor:

PANDYA Ashish A, 4318 Lafayette Drive, El Dorado Hills, CA 95762, US, US
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Legal Representative:

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Patent and Priority Information (Country, Number, Date):

Patent: WO 2003104943 A2 20031218 (WO 03104943)

Application: WO 2003US18386 20030610 (PCT/WO US0318386)

Priority Application: US 2002388407 20020611

Designated States:

(Protection type is "patent" unless otherwise stated - for applications
prior to 2004)

AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ
EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR
LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SC SD SE SG
SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZM ZW

(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT RO SE
SI SK TR

(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG

(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English

Filing Language: English

Fulltext Word Count: 56454

Fulltext Availability:

Detailed Description

Detailed Description

... a high performance routing engine, a high performance network
management engine, deep packet inspection engine providing string search,
an engine for XML, an engine for **virtualization**, and the like, 0
providing support for an application specific acceleration. The
processing capability of this IP processor can be scaled by scaling the
number of SAN Packet **Processor blocks** 1706 (a) through 1706 (n) in
the chip to meet the line rate requirements of the network interface. The
primary limitation from the scalability would...

1/3,K/10 (Item 10 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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01060886

CONTROL REGISTER ACCESS VIRTUALIZATION PERFORMANCE IMPROVEMENT IN THE
VIRTUAL-MACHINE ARCHITECTURE
ARCHITECTURE DE MACHINE VIRTUELLE: AMELIORATION DES PERFORMANCES DE
VIRTUALISATION DE L'ACCES AU REGISTRE DE COMMANDE

Patent Applicant/Assignee:

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Legal Representative:

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Patent and Priority Information (Country, Number, Date):

Patent: WO 200390070 A2-A3 20031030 (WO 0390070)
Application: WO 2003US9482 20030327 (PCT/WO US03009482)
Priority Application: US 2002124641 20020416

Designated States:

(Protection type is "patent" unless otherwise stated - for applications
prior to 2004)

AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ
EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR
LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SC SD SE SG
SK SL TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT RO SE
SI SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English

Filing Language: English

Fulltext Word Count: 7129

Fulltext Availability:

Detailed Description

Detailed Description

... the shadow value field combined with values from the actual register
resource for portions of the resource that are under guest control to
guest software (**processing block** 414).

[00401 One embodiment in which the transfer of control to the VMM is
supported via VMX operation discussed in greater detail above with
reference to Figure I will now be described in more detail.

[0041]In one embodiment, the VMM maintains a set of control bits to
configure which **virtualization** events will cause a VIVI exit. This set
of control bits is referred to herein as a redirection map. In one

embodiment, the redirection
map...

...run on a general purpose computer system or a dedicated machine), or a combination of both.

[0044] Referring to Figure 5, process 500 begins at **processing block 502**

with processing logic identifying an occurrence of a **virtualization** event caused by a request of guest software to access a portion of a hardware resource such as a control register. This request is either...

...one or more portions of a particular register or a command to write data to one or more portions of a particular register.

[0045]At **processing block 503**, processing logic consults the redirection

map to determine if the unconditional exit bit associated with this **virtualization** event is set (decision box 506). If this bit is set, processing logic triggers a VM exit (**processing block 522**). For example, in the IA-32 ISA the redirection map may include bits to unconditionally cause VM exits on writes to CR2, reads from...

1/3,K/11 (Item 11 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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01051319 **Image available**

**METHOD, SYSTEM, AND PROGRAM FOR AN IMPROVED ENTERPRISE SPATIAL SYSTEM
PROCEDE, SYSTEME ET LOGICIEL POUR UN SYSTEME SPATIAL AMELIORE D'ENTREPRISE**

Patent Applicant/Assignee:

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Patent and Priority Information (Country, Number, Date):

Patent: WO 200381388 A2-A3 20031002 (WO 0381388)
Application: WO 2003US8296 20030317 (PCT/WO US03008296)
Priority Application: US 2002364807 20020316

Designated States:

(Protection type is "patent" unless otherwise stated - for applications
prior to 2004)

AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ
EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR
LS LT LU LV MA MD MG MK MN MW MX MZ NI NO NZ OM PH PL PT RO RU SC SD SE
SG SK SL TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT RO SE
SI SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English

Filing Language: English

Fulltext Word Count: 108397

Fulltext Availability:

Detailed Description

Detailed Description

... registration process for transaction-based users in accordance with
certain implementations of the invention. Control begins at block
5810withaWelcomeUIScreenbeingdisplayedtotheuser. Inblock5812,ifa
continue button is selected, **processing** continues to **block** 5814,
otherwise, if a cancel button has been selected, **processing** continues
to **block** 5830. In block 5814, user
logininformationiscollectedviaaregistrationUIScreen. Inblock5816,ifa
continue button was selected, **processing** continues to **block** 5818,
otherwise, if a cancel button has been selected, processing continues to
block 5843. In block 5818, it is detennined whether there is an error...

1/3,K/12 (Item 12 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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01045186 **Image available**

**STORAGE VIRTUALIZATION SYSTEM CONVERSION MANAGEMENT APPARATUS AND STORAGE
VIRTUALIZATION SYSTEM CONVERSION MANAGEMENT METHOD
DISPOSITIF ET PROCEDE DE GESTION DE CONVERSION DE SYSTEME DE VIRTUALISATION
DE MEMOIRE**

Patent Applicant/Assignee:

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Patent and Priority Information (Country, Number, Date):

Patent: WO 200375161 A1 20030912 (WO 0375161)

Application: WO 2002JP2143 20020307 (PCT/WO JP0202143)

Priority Application: WO 2002JP2143 20020307

Designated States:

(Protection type is "patent" unless otherwise stated - for applications
prior to 2004)

JP US

(EP) DE GB

Publication Language: Japanese

Filing Language: Japanese

English Abstract

A conversion control block (2) relates a virtual memory address to the actual memory address of each storage apparatus, so as to set a storage **virtualization** apparatus in charge, delivers the relationship between the virtual memory address and the actual memory address handled by each storage **virtualization** apparatus as storage conversion tables (21, 22, 23) to the storage **virtualization** apparatuses, and delivers the relationship between the virtual memory address and the storage apparatus in charge as a routing table (11) to servers. Furthermore, a load monitoring block and a load dispersion **processing block** provided in each storage **virtualization** apparatus monitor the load, a failure recovery **processing block** detects failure of the storage **virtualization** apparatus, so that memory address conversion handled by the storage **virtualization** apparatus where load is concentrated or failure has occurred is allocated in another storage **virtualization** apparatus.

1/3,K/13 (Item 13 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00922970 **Image available**

METHOD FOR RESOLVING ADDRESS SPACE CONFLICTS BETWEEN A VIRTUAL MACHINE
MONITOR AND A GUEST OPERATING SYSTEM

PROCEDE DE RESOLUTION DE CONFLITS D'ESPACES ADRESSES ENTRE UN MONITEUR DE
MACHINE VIRTUELLE ET UN SYSTEME D'EXPLOITATION INVITE

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Patent and Priority Information (Country, Number, Date):

Patent: WO 200256172 A2-A3 20020718 (WO 0256172)

Application: WO 2001US50415 20011220 (PCT/WO US2001050415)

Priority Application: US 2000752587 20001227

Designated States:

(Protection type is "patent" unless otherwise stated - for applications
prior to 2004)

AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ
EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR
LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK
SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG

(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English

Filing Language: English

Fulltext Word Count: 6059

Fulltext Availability:

Detailed Description

Detailed Description

... as described in greater 1 5 detail above in conjunction with Figure 4.

Figure 6 is a flow diagram of a method 600 for handling **virtualization**
traps generated by a guest OS, according to one embodiment of the present
invention. Method 600 begins with setting access rights of the region
occupied by the VMK to a more privileged level than a privilege level
associated with the guest OS (**processing block 604**). For instance,
all VMK pages may

1/3,K/14 (Item 14 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2006 WIPO/Univentio. All rts. reserv.

00919210 **Image available**
PROCESSOR MODE FOR LIMITING THE OPERATION OF GUEST SOFTWARE RUNNING ON A
VIRTUAL MACHINE SUPPORTED BY A MONITOR
NOUVEAU MODE PROCESSEUR DESTINE A LIMITER LE FONCTIONNEMENT D'UN LOGICIEL
INVITE S'EXECUTANT SUR UNE MACHINE VIRTUELLE MISE EN OEUVRE PAR UN
MONITEUR MACHINE VIRTUELLE

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COTA-ROBLES Erik, 4238 SW Marigold, Portland, OR 97219, US,
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Patent and Priority Information (Country, Number, Date):

Patent: WO 200252404 A2-A3 20020704 (WO 0252404)
Application: WO 2001US45061 20011127 (PCT/WO US0145061)
Priority Application: US 2000752134 20001227

Designated States:

(Protection type is "patent" unless otherwise stated - for applications
prior to 2004)

AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ
EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR
LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK
SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG

(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English

Filing Language: English

Fulltext Word Count: 6330

Fulltext Availability:

Detailed Description

Detailed Description

... this attempt, V32 mode is exited to transfer control over the
operation initiated by the guest software to the VMM which runs outside
V32 mode (**processor block** 408). In one

14

embodiment, the VMM configures what operations should cause a transition
out of V32 mode as will be described in greater detail below in
conjunction with Figure 7. In one embodiment, such operations generate
virtualization traps that cause a transition out of V32 mode.

Alternatively, any other mechanism known in the art can be used to cause
a transition outwith identifying an attempt of guest software to perform
an operation that may be
restricted by V32 mode (**processing block** 604). At decision box 606, a

I 0 determination is made as to whether the attempt of the guest software can potentially succeed. If the determination is positive, a **virtualization** trap is generated (**processing block 608**). Alternatively, no **virtualization** trap is generated, and the guest software proceeds with the operation (**processing block 610**). For instance, according to the IA-32 ISA, the RDMSR instruction can be 1 5 executed only by software running with supervisor privilege. Consequently ...

...the present invention. According to this embodiment, the VMM maintains a redirection map to configure which interrupts and exceptions should result in a virtualization trap (**processing block 704**). At **processing block 706**, an occurrence of an interrupt or exception is identified. The

17 redirection map is then consulted to find a bit associated with this interrupt or exception in the redirection bitmap (**processing block 708**).

At decision box 710, a determination is made as to whether this interrupt is allowed to be handled by the guest OS. If the determination is positive, the interrupt or exception is delivered to V32 mode and is handled by the guest OS (**processing block 714**). Alternatively, a **virtualization** trap is generated, causing a transition out of V32 mode (**processing block 712**).

Figure 8 is a flow diagram of a method 800 for controlling masking of interrupts, according to one embodiment of the present invention. Various ...

...prevented from accessing the interrupt flag by providing a shadow interrupt flag (e.g., EFLAGS.VMIF) for modifications by the guest software, by generating a **virtualization** trap in response to such an attempt of the guest software, or by using any other technique known in the art.

Method 800 begins with identifying an attempt of guest software to modify an interrupt flag that may potentially control masking of interrupts (**processing**

1 8 **block 804**). At decision box 806, a determination is made as to whether the interrupt flag controls the masking of interrupts. If the determination is negative...

...shadow flag (decision box 810). If the determination is negative, i.e., I 0 the guest software attempts to modify the actual interrupt flag, a **virtualization** trap occurs (**processing block 812**), causing a transition out of V32 mode (**processing block 816**). Alternatively, if the actual interrupt flag is not accessible to the guest software, the guest software is allowed to modify the shadow interrupt flag (**processing block 814**).

1 5 Figure 9 is a block diagram of one embodiment of a processing system.

Processing system 900 includes processor 920 and memory 930...

1/3,K/15 (Item 15 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00891805 **Image available**

A METHOD OF AUDIO SIGNAL PROCESSING FOR A LOUDSPEAKER LOCATED CLOSE TO AN EAR

PROCEDE POUR TRAITER DES SIGNAUX SONORES POUR UN HAUT-PARLEUR SITUE PRES DE L'OREILLE DE L'AUDITEUR

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Patent and Priority Information (Country, Number, Date):

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Application: WO 2001GB4055 20010910 (PCT/WO GB0104055)

Priority Application: GB 200022891 20000919

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GB JP

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

Publication Language: English

Filing Language: English

Fulltext Word Count: 8052

Fulltext Availability:

Detailed Description

Detailed Description

... iterative process continues ad infinitum, creating successive orders of simulated reflections 2,3, 4...

and so on, with decaying amplitude. By creating several delay-line **processing blocks** according to Figure 2, having differing characteristics corresponding

0 0 0

respectively to room width, height and length, then it is possible to cross-link them for a more sophisticated reflections simulation.

If such simulated sound reflections and reverberation are added to the **virtualisation** processing (Figure 4), then the externalisation effect can be improved a little, but nowhere near as much as might be expected from such careful calculation...the two derivative complementary filters are different in terms of detail. This decorrelated pair is more effective for creating externalisation when symmetry exists in the **virtualisation** arrangements, for example, when virtualising the centre channel of a "5.1" channel movie surround system.

There are two basic options for incorporating the invention into an HRTFbased **virtualisation**. Firstly, a single wave-scattering filter can be incorporated serially into the input port of the HRTF **processing block**, as shown in Figure 13 (lower). This is economical in terms of processing load, although not quite so effective as the complementary pair configuration (next...

File 8: Ei Compendex(R) 1970-2006/Jun W2
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 (c) 2006 Japan Science and Tech Corp(JST)
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 File 434: SciSearch(R) Cited Ref Sci 1974-1989/Dec
 (c) 1998 Inst for Sci Info
 File 34: SciSearch(R) Cited Ref Sci 1990-2006/Jun W3
 (c) 2006 Inst for Sci Info
 File 99: Wilson Appl. Sci & Tech Abs 1983-2006/May
 (c) 2006 The HW Wilson Co.
 File 583: Gale Group Globalbase(TM) 1986-2002/Dec 13
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 File 266: FEDRIP 2005/Dec
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 File 62: SPIN(R) 1975-2006/Apr W1
 (c) 2006 American Institute of Physics
 File 239: Mathsci 1940-2006/Jul
 (c) 2006 American Mathematical Society

Set	Items	Description
S1	2	(PROCESS???(2W)BLOCK? ?)(50N)(VIRTUALI?AT?)

1/3,K/1 (Item 1 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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07041715 E.I. No: EIP04408382526

Title: SANBoost: Automated SAN-level caching in storage area networks
Author: Ari, Ismail; Gottwals, Melanie; Henze, Dick
Corporate Source: Storage Systems Research Center University of
California, Santa Cruz, CA, United States
Conference Title: Proceedings - International Conference on Autonomic
Computing
Conference Location: New York, NY, United States Conference Date:
20040517-20040518
E.I. Conference No.: 63507
Source: Proceedings - International Conference on Autonomic Computing
Proceedings - International Conference on Autonomic Computing 2004.
Publication Year: 2004
ISBN: 0769521142
Language: English

...Abstract: basis to provide a performance isolation mechanism for
response time metrics related to storage quality of service (QoS).
SANBoost automates hot data detection and migration **processes** in **block**
-level storage. The design consists of a migration module implemented in a
fabric-based SAN **virtualization** appliance and a Solid-State Disk (SSD)
that acts as a cache resource within the same SAN. Simulation results
quantify the impact of a specific...

1/3,K/2 (Item 1 from file: 2)

DIALOG(R)File 2:INSPEC

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09047797 INSPEC Abstract Number: C2004-09-5320G-018

Title: SANBoost: automated SAN-level caching in storage area network

Author(s): Ari, I.; Gottwals, M.; Henze, D.

Author Affiliation: Storage Syst. Res. Center, California Univ., Santa Cruz, CA, USA

Conference Title: Proceedings of the First International Conference on Autonomic Computing p.164-71

Publisher: IEEE Comput. Soc, Los Alamitos, CA,USA

Publication Date: 2004 Country of Publication: USA xv+343 pp.

ISBN: 0 7695 2114 2 Material Identity Number: XX-2004-01309

U.S. Copyright Clearance Center Code: 0-7695-2114-2/04/\$20.00

Conference Title: Proceedings of the First International Conference on Autonomic Computing

Conference Date: 17-18 May 2004 Conference Location: New York, NY, USA

Language: English

Subfile: C

Copyright 2004, IEE

...Abstract: basis to provide a performance isolation mechanism for response time metrics related to storage quality of service (QoS). SANBoost automates hot data detection and migration **processes** in **block**-level storage. The design consists of a migration module implemented in a fabric-based SAN **virtualization** appliance and a solid-state disk (SSD) that acts as a cache resource within the same SAN. Simulation results quantify the impact of a specific...

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 File 275:Gale Group Computer DB(TM) 1983-2006/Jun 20
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 File 160:Gale Group PROMT(R) 1972-1989
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 File 370:Science 1996-1999/Jul W3
 (c) 1999 AAAS
 File 148:Gale Group Trade & Industry DB 1976-2006/Jun 21
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 File 634:San Jose Mercury Jun 1985-2006/Jun 20
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 File 88:Gale Group Business A.R.T.S. 1976-2006/Jun 13
 (c) 2006 The Gale Group

Set	Items	Description
S1	5	(PROCESS???(2W)BLOCK? ?)(50N)(VIRTUALI?AT?)

1/3,K/1 (Item 1 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
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02184850 73943258

Pirus is switching on convergence

Fass, Ilona

Computer Technology Review v21n5 PP: 58 May 2001

ISSN: 0278-9647 JRNL CODE: CTN

WORD COUNT: 1235

...TEXT: computational elements, and then to be connected to ports is a very interesting architecture fundamentally.

And when you take that platform and apply sophisticated TCP **processing** , FC **processing** , **block virtualization** , file system technology, and the ability to translate FC to iSCSI or iSCSI to FC, you have a next generation platform that is fundamentally a...

1/3,K/2 (Item 1 from file: 610)
DIALOG(R)File 610:Business Wire
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0001181394 I56C49860281111D9A995B07AB4E12F4C (USE FORMAT 7 FOR FULLTEXT)
**Maranti Achieves Unparalleled Protocol Processing Performance Utilizing
AMCC's Network Processor Solutions**

Business Wire

Wednesday, October 27, 2004 T12:01:00Z

JOURNAL CODE: BW LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT

DOCUMENT TYPE: NEWSWIRE

WORD COUNT: 896

...s solutions through multiple generations of network processor
development.

Utilizing AMCC's nP7250 network processor, Maranti's storage controllers have demonstrated unparalleled deep in-band **virtualization** protocol processing and storage replication application performance. Current testing, independently validated by the Tolly Group, has demonstrated throughput results of more than 200K IOPS on a single port, with scalability to millions of IOPS across the CoreSTOR platforms. Maranti's deep in-band storage **virtualization processes** SCSI **block** read and write commands with no control path processing and an un-buffered, cut-through data path architecture, which is unique among all SAN storage **virtualization** products.

"We have a long and successful history of working with AMCC and regard them as a market and technology leader in the network processor...

1/3,K/3 (Item 1 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)
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03833674 Supplier Number: 123667849 (USE FORMAT 7 FOR FULLTEXT)
**Maranti Achieves Unparalleled Protocol Processing Performance Utilizing
AMCC's Network Processor Solutions.**

Business Wire, pNA

Oct 27, 2004

Language: English Record Type: Fulltext

Document Type: Newswire; Trade

Word Count: 914

... s solutions through multiple generations of network processor development.

Utilizing AMCC's nP7250 network processor, Maranti's storage controllers have demonstrated unparalleled deep in-band **virtualization** protocol processing and storage replication application performance. Current testing, independently validated by the Tolly Group, has demonstrated throughput results of more than 200K IOPS on a single port, with scalability to millions of IOPS across the CoreSTOR platforms. Maranti's deep in-band storage **virtualization processes** SCSI **block** read and write commands with no control path processing and an un-buffered, cut-through data path architecture, which is unique among all SAN storage **virtualization** products.

"We have a long and successful history of working with AMCC and regard them as a market and technology leader in the network processor...

1/3,K/4 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
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11584129 Supplier Number: 123667849 (USE FORMAT 7 FOR FULLTEXT)
**Maranti Achieves Unparalleled Protocol Processing Performance Utilizing
AMCC's Network Processor Solutions.**

Business Wire, pNA

Oct 27, 2004

Language: English Record Type: Fulltext

Document Type: Newswire; Trade

Word Count: 914

... s solutions through multiple generations of network processor development.

Utilizing AMCC's nP7250 network processor, Maranti's storage controllers have demonstrated unparalleled deep in-band **virtualization** protocol processing and storage replication application performance. Current testing, independently validated by the Tolly Group, has demonstrated throughput results of more than 200K IOPS on a single port, with scalability to millions of IOPS across the CoreSTOR platforms. Maranti's deep in-band storage **virtualization processes** SCSI **block** read and write commands with no control path processing and an un-buffered, cut-through data path architecture, which is unique among all SAN storage **virtualization** products.

"We have a long and successful history of working with AMCC and regard them as a market and technology leader in the network processor...

1/3,K/5 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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0017550939 SUPPLIER NUMBER: 123667849 (USE FORMAT 7 OR 9 FOR FULL
TEXT)

**Maranti Achieves Unparalleled Protocol Processing Performance Utilizing
AMCC's Network Processor Solutions.**

Business Wire, NA

Oct 27, 2004

LANGUAGE: English RECORD TYPE: Fulltext

WORD COUNT: 914 LINE COUNT: 00082

... s solutions through multiple generations of network processor
development.

Utilizing AMCC's nP7250 network processor, Maranti's storage
controllers have demonstrated unparalleled deep in-band **virtualization**
protocol processing and storage replication application performance.
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demonstrated throughput results of more than 200K IOPS on a single port,
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Maranti's deep in-band storage **virtualization processes** SCSI **block**
read and write commands with no control path processing and an un-buffered,
cut-through data path architecture, which is unique among all SAN storage
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"We have a long and successful history of working with AMCC and
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Set	Items	Description
S1	18087	(SOFTWARE OR PROGRAM? ? OR APPLICATION? ? OR CODE? ? OR GAME? ? OR APPLET? ? OR THREAD? ? OR MULTITHREAD? ? OR MULTI()THREAD? ? OR FILE? ? OR APP OR APPS OR MACRO? ? OR SCRIPT? OR - BROWSER? OR WEBBROWSER? OR SUBROUTIN? OR SUBPROGRAM? OR OS OR OPERATING()SY
S2	11566194	(SOFTWARE OR PROGRAM? ? OR APPLICATION? ? OR CODE? ? OR GAME? ? OR APPLET? ? OR THREAD? ? OR MULTITHREAD? ? OR MULTI()THREAD? ? OR FILE? ? OR APP OR APPS OR MACRO? ? OR SCRIPT? OR - BROWSER? OR WEBBROWSER? OR SUBROUTIN? OR SUBPROGRAM? OR OS OR OPERATING()SY
S3	344616	S2(5N) (CONVERT??? OR ADJUST???? OR CHANG??? OR ADAPT? OR C-ONVERSION? OR ALTER??? OR MODIFY??? OR TRANSLAT? OR TRANSFORM? OR MODIFICATION? ?)
S4	113486	DATASTRUCTUR??? OR DATA()STRUCTUR???
S5	4875	PROCESS??? (2W)BLOCK? ?
S6	7	S4(20N)S5
S7	0	S1(30N)S6
S8	0	S3(30N)S6
S9	7	S1(30N)S5
S10	225	S3(30N)S5
S11	1360	S5(50N)S2
S12	4513577	(METHOD? OR ACTION? ? OR COURSE? ? OR EVOLUTION OR FORMATI-ON? ? OR FORM??? OR MANNER? ? OR MECHANISM? ? OR MODE? ? OR O-PERAT???) (30N) (PLAN OR CHARACTERI? OR CHART??? OR DESCRI? OR -LAY()OUT OR LAYOUT)
S13	3897520	(METHOD? OR ACTION? ? OR COURSE? ? OR EVOLUTION OR FORMATI-ON? ? OR FORM??? OR MANNER? ? OR MECHANISM? ? OR MODE? ? OR O-

PERAT???) (30N) (PLOT? ? OR PLOTTING OR ARRANG? OR BLUEPRINT? ?
OR CALCULAT? OR DESIGN?)

S14 1923559 (METHOD? OR ACTION? ? OR COURSE? ? OR EVOLUTION OR FORMATI-
ON? ? OR FORM??? OR MANNER? ? OR MECHANISM? ? OR MODE? ? OR O-
PERAT???) (30N) (FORMULAT? OR FRAM??? OR MAP???? OR ORGANI?AT? -
OR ORGANI???? OR OUTLIN???)

S15 3350262 (METHOD? OR ACTION? ? OR COURSE? ? OR EVOLUTION OR FORMATI-
ON? ? OR FORM??? OR MANNER? ? OR MECHANISM? ? OR MODE? ? OR O-
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? OR CONSTITUENT? ? OR DETAIL???)

S16 770740 (METHOD? OR ACTION? ? OR COURSE? ? OR EVOLUTION OR FORMATI-
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PERAT???) (30N) (MODULE? ? OR SECTION? ? OR SEGMENT? ?)

S17 3381857 (PROCEDURE? ? OR PROCEEDING? ? OR PROGRESS??? OR PROGRESSI-
ON? ? OR ROUTINE? ? OR SUBROUTINE? ? OR RULE? ? OR STAGE? ? OR
STEP? ? OR SYSTEM? ? OR TECHNIQUE? ?) (30N) (PLAN OR CHARACTER-
I? OR CHART??? OR DESCRI? OR LAY()OUT OR LAYOUT)

S18 2879589 (PROCEDURE? ? OR PROCEEDING? ? OR PROGRESS??? OR PROGRESSI-
ON? ? OR ROUTINE? ? OR SUBROUTINE? ? OR RULE? ? OR STAGE? ? OR
STEP? ? OR SYSTEM? ? OR TECHNIQUE? ?) (30N) (PLOT? ? OR PLOTTI-
NG OR ARRANG? OR BLUEPRINT? ? OR CALCULAT? OR DESIGN?)

S19 1354243 (PROCEDURE? ? OR PROCEEDING? ? OR PROGRESS??? OR PROGRESSI-
ON? ? OR ROUTINE? ? OR SUBROUTINE? ? OR RULE? ? OR STAGE? ? OR
STEP? ? OR SYSTEM? ? OR TECHNIQUE? ?) (30N) (FORMULAT? OR FRAM-
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S20 2356161 (PROCEDURE? ? OR PROCEEDING? ? OR PROGRESS??? OR PROGRESSI-
ON? ? OR ROUTINE? ? OR SUBROUTINE? ? OR RULE? ? OR STAGE? ? OR
STEP? ? OR SYSTEM? ? OR TECHNIQUE? ?) (30N) (REPRESENT? OR SCH-
EM??? OR CONSTRUCT??? OR UNIT? ? OR CONSTITUENT? ? OR DETAIL?-
??)

S21 537429 (PROCEDURE? ? OR PROCEEDING? ? OR PROGRESS??? OR PROGRESSI-
ON? ? OR ROUTINE? ? OR SUBROUTINE? ? OR RULE? ? OR STAGE? ? OR
STEP? ? OR SYSTEM? ? OR TECHNIQUE? ?) (30N) (MODULE? ? OR SECT-
ION? ? OR SEGMENT? ?)

S22 4016 S12:S21(30N)S1

S23 83635 S12:S21(30N)S3

S24 5 S22(50N)S5

S25 34 S23(50N)S5

S26 1371 VIRTUALI?AT?

S27 10 S26(50N)S1

S28 28 S26(50N)S3

S29 0 S25(50N)S28

9/7/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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06646952 E.I. No: EIP03497767784

Title: Image compression coder selection and specific implementations in
a COTS versus custom software/hardware environment

Author: Allen, John D.

Corporate Source: Raytheon Technical Services Company, Indianapolis, IN,
United States

Conference Title: The 22nd Digital Avionics Systems Conference -
Proceedings

Conference Location: Indianapolis, IN, United States Conference Date:
20031012-20031016

Sponsor: IEEE; AIAA

E.I. Conference No.: 61847

Source: AIAA/IEEE Digital Avionics Systems Conference - Proceedings v 2
2003. p 10.B.5/1-10.B.5/13 (IEEE cat n 03CH37449)

Publication Year: 2003

CODEN: ADACFY

Language: English

Document Type: CA; (Conference Article) Treatment: T; (Theoretical)

Journal Announcement: 0312W3

Abstract: A generalized model for transform-based image compression
applications was developed, and desired properties for each of the model
processing blocks were identified. By identifying specific techniques
to address each of the transform, quantization and encoding processes, a
software implementation was developed. The **software** implementation was
then "**ported**" to a strictly COTS hardware environment. Additional
requirements were proposed for the hardware, such as time-critical video
applications. (Edited abstract) 9 Refs.

9/7/2 (Item 2 from file: 8)
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02077713 E.I. Monthly No: EIM8603-015077

Title: FUNCTIONAL MAPPING FOR MICROPROCESSOR SYSTEM SIMULATION.

Author: Marshall, W. K.; Zobrist, G. W.; Bach, W.; Richardson, A.

Corporate Source: Univ of Missouri at Rolla, Graduate Engineering Cent,
St. Louis, MO, USA

Conference Title: 1985 IEEE Microprocessor Forum: Design Productivity
Through Engineering Workstations.

Conference Location: Atlantic City, NJ, USA Conference Date: 19850402

Sponsor: IEEE Computer Soc, Los Alamitos, CA, USA.; IEEE, New York, NY,
USA.

E.I. Conference No.: 07657

Source: Publ by IEEE, New York, NY, USA Available from IEEE Service Cent
(Cat n 85CH2151-9), Piscataway, NJ, USA p 15-19

Publication Year: 1985

ISBN: 0-8186-0616-9

Language: English

Document Type: PA; (Conference Paper)

Journal Announcement: 8603

Abstract: The object code portion of a microprocessor must be modeled in order to functionally simulate a microprocessor-based electronic system. The automated technique presented here for creating functionally equivalent high-level **programs** for the executable **portion** of the **software** represents one step towards the total automation of the simulation model building **process**. The **block** primitives provide a convenient way to simulate sections of the microcode rather than individual statements. The instruction timing preserved for each block can be incorporated into the simulation in order to maintain timing resolution with respect to other simulation models. The table-lookup-driven translation scheme makes switching possible between a variety of simulation languages with minimal changes to the translator software. 6 refs.

9/7/3 (Item 1 from file: 2)

DIALOG(R)File 2:INSPEC

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08992445 INSPEC Abstract Number: B2004-07-6135C-341, C2004-07-1250M-074

Title: Image compression coder selection and specific implementations in a cots versus custom software/hardware environment

Author(s): Allen, J.D.

Author Affiliation: Raytheon Tech. Services Co., Indianapolis, IN, USA

Conference Title: 22nd Digital Avionics Systems Conference. Proceedings
(Cat. No.03CH37449) Part vol.2 p.10.B.5-1-13 vol.2

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 2003 Country of Publication: USA 2
vol.(xxx+xiii+664+838) pp.

ISBN: 0 7803 7844 X Material Identity Number: XX-2003-03334

U.S. Copyright Clearance Center Code: 0 7803 7844 X/2003/\$17.00

Conference Title: 22nd Digital Avionics Systems Conference. Proceedings

Conference Date: 12-16 Oct. 2003 Conference Location: Indianapolis,
IN, USA

Medium: Also available on CD-ROM in PDF format

Language: English Document Type: Conference Paper (PA)

Treatment: Applications (A); Practical (P); Theoretical (T)

Abstract: This paper presents a generalized model for transform-based image compression applications and identified desired properties for each of the model **processing blocks**. By identifying specific techniques to address each of the transform, quantization and encoding process, a software implementation was developed. The **software** implementation was then "**ported**" to a strictly COTS hardware environment. (9 Refs)

Subfile: B C

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9/7/4 (Item 2 from file: 2)

DIALOG(R)File 2:INSPEC

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04560741 INSPEC Abstract Number: B90014148, C90013158

Title: Custom DSP chip extends instrument capabilities

Author(s): Kareen, A.

Author Affiliation: Tektronix, Beaverton, UK

Journal: Electronic Product Design vol.10, no.9 p.41-4, 47

Publication Date: Oct. 1989 Country of Publication: UK

CODEN: EPDEDB ISSN: 0263-1474

Language: English Document Type: Journal Paper (JP)

Treatment: Practical (P); Product Review (R)

Abstract: The test and measurement industry has already embraced DSP for new product concepts as well as for enhancing the capabilities of their existing product offering. A block diagram of a typical DSP based system is shown. The TriStar single-chip programmable digital signal processor uses a Harvard architecture, prefetched instructions, wide instruction word, two external data memories, and extensive parallelism to provide high performance and throughput in waveform processing. Although its architecture has been optimised for test instruments, the TriStar is capable of performing general digital signal **processing** tasks. The **block** diagram of the processor is shown. The chip includes a 16*32 bit three-**port** data register **file**, four 16*20 bit address register files, and a 16*20 bit instruction address stack. These elements are organised to form three major units: an arithmetic unit (AU), an address computation unit (ACU), and an instruction fetch unit (IFU), which all operate in parallel. The TriStar is a single cycle machine with all instructions executed in 150 nsec cycle time. The two Data memories and the instruction memory are separated to allow for simultaneous fetching of instructions and accessing of data. Communications between the units is via status flags and a register Bus. The AU internal data path is 32 bits wide allowing execution of many double precision (32 bit) operations. (0 Refs)

Subfile: B C

9/7/5 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2006 Institution of Electrical Engineers. All rts. reserv.

03586819 INSPEC Abstract Number: C86010777

Title: A functional mapping for microprocessor system simulation

Author(s): Marshall, W.K.; Zobrist, G.W.; Bach, W.; Richardson, A.

Author Affiliation: Graduate Eng. Center, Missouri Univ., Rolla, MO, USA

Conference Title: 1985 IEEE Microprocessor Forum (Design Productivity Through Engineering Workstations) (Cat. No. 85CH2151-9) p.15-19

Publisher: IEEE Comput. Soc. Press, Silver Spring, MD, USA

Publication Date: 1985 Country of Publication: USA x+181 pp.

ISBN: 0 8186 0616 9

U.S. Copyright Clearance Center Code: CH2151-9/85/0000-0015\$01.00

Conference Sponsor: IEEE

Conference Date: 2-4 April 1985 Conference Location: Atlantic City, NJ, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: The object code portion of a microprocessor must be modeled in order to functionally simulate a microprocessor-based electronic system. The automated technique presented here for creating functionally equivalent high-level **programs** for the executable **portion** of the **software** represents one step towards the total automation of the simulation model building **process**. The **block** primitives provide a convenient way to simulate sections of the microcode rather than individual statements. The instruction timing preserved for each block can be incorporated into the simulation in order to maintain timing resolution with respect to other simulation models. The table-lookup-driven translation scheme makes switching possible between a variety of simulation languages with minimal changes to the translator software. (6 Refs)

Subfile: C

9/7/6 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC
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02319529 INSPEC Abstract Number: C79009900

**Title: Closing the software gap for interactive mini/microcomputation:
direct execution of microprogrammed block-diagram primitives**

Author(s): Korn, G.A.

Author Affiliation: Univ. of Arizona, Tucson, AZ, USA

Conference Title: Proceedings of COMPSAC 78 Computer Software and
Applications Conference p.93-103

Publisher: IEEE, New York, NY, USA

Publication Date: 1978 Country of Publication: USA xiv+832 pp.

Conference Sponsor: IEEE

Conference Date: 13-16 Nov. 1978 Conference Location: Chicago, IL, USA

Language: English Document Type: Conference Paper (PA)

Treatment: General, Review (G)

Abstract: Block-diagram programs, for instrumentation, control, and simulation systems are especially easy to translate, since no explicit precedence analysis is needed. Block-diagram primitives range from simple adders to complete real-time controllers. They are pure-procedure, reentrant microprograms or threaded code in read-only memory, which may be pre-programmed and plugged in for special applications. In addition to hand 'assembly' and optimizing compilation of the block-diagram programs, the author exhibits the direct-executive MICRODARE II system, which embeds block-diagram 'assembly' in an advanced BASIC dialect serving for interactive editing, job control, and file manipulation. Execution speeds of the systems permit LSI 11 microcomputers and PDP 11 minis to match and exceed those of a CDC 6400; a number of examples are shown. The report continues with a discussion of future multi-task, multiprocessor real-time BASIC systems incorporating MICRODARE. The author finally describes a new two-processor system consisting of an LSI-11 running MICRODARE **software** joined by a two- **port** memory to an ultra-fast bit-sliced 2903/2910 **processor** executing **block** -diagram microprograms. (13 Refs)

Subfile: C

9/7/77 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS
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0687226 NTIS Accession Number: FE-2275-4/XAB

**Systems Studies of Coal Conversion Processes Using a Reference Simulator.
Quarterly Report, April 1, 1977--June 30, 1977**

Reklaitis, G. V. ; Woods, J. M. ; Kayihan, F. ; Sood, M.

Purdue Univ., Lafayette, Ind.

Corp. Source Codes: 5347000

Sponsor: Department of Energy.

Jul 77 41p

Journal Announcement: GRAI7812; NSA0300

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NTIS Prices: PC A03/MF A01

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Preliminary user's manuals were prepared for the physical properties code package and for the **process block** material balancing code. These **codes** together with a major **portion** of the process equipment calculation system were released to ORNL, Lehigh University, and ERDA-Aberdeen. Significant process has been made in the pyrolysis section model and on the process equipment calculation system. Manuals for these codes are under preparation. The equipment calculation system has been linked with the properties package and expansion of the module library is proceeding. Development work has continued on the equipment costing system and the hydrotreating models. The cost data files have been implemented on the computer and work is in progress on the file manipulation and costing subroutines. Literature review is complete on the hydrotreating section and semi-empirical model equations have been assembled and fitted to available data. Further flowsheet modelling will be suspended until a base case flowsheet is developed. (ERA citation 03:013635)

24/7/1 (Item 1 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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02077713 E.I. Monthly No: EIM8603-015077

Title: **FUNCTIONAL MAPPING FOR MICROPROCESSOR SYSTEM SIMULATION.**

Author: Marshall, W. K.; Zobrist, G. W.; Bach, W.; Richardson, A.

Corporate Source: Univ of Missouri at Rolla, Graduate Engineering Cent,
St. Louis, MO, USA

Conference Title: 1985 IEEE Microprocessor Forum: Design Productivity
Through Engineering Workstations.

Conference Location: Atlantic City, NJ, USA Conference Date: 19850402

Sponsor: IEEE Computer Soc, Los Alamitos, CA, USA.; IEEE, New York, NY,
USA.

E.I. Conference No.: 07657

Source: Publ by IEEE, New York, NY, USA Available from IEEE Service Cent
(Cat n 85CH2151-9), Piscataway, NJ, USA p 15-19

Publication Year: 1985

ISBN: 0-8186-0616-9

Language: English

Document Type: PA; (Conference Paper)

Journal Announcement: 8603

Abstract: The object **code portion** of a microprocessor must be modeled in order to functionally simulate a microprocessor-based electronic **system**. The automated technique presented here for creating functionally equivalent high-level **programs** for the executable **portion** of the **software represents** one **step** towards the total automation of the simulation **model building process**. The **block** primitives provide a convenient way to simulate **sections** of the microcode rather than individual statements. The instruction timing preserved for each block can be incorporated into the simulation in order to maintain timing resolution with respect to other simulation models. The table-lookup-driven translation scheme makes switching possible between a variety of simulation languages with minimal changes to the translator software. 6 refs.

24/7/2 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
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04560741 INSPEC Abstract Number: B90014148, C90013158

Title: Custom DSP chip extends instrument capabilities

Author(s): Kareen, A.

Author Affiliation: Tektronix, Beaverton, UK

Journal: Electronic Product Design vol.10, no.9 p.41-4, 47

Publication Date: Oct. 1989 Country of Publication: UK

CODEN: EPDEDB ISSN: 0263-1474

Language: English Document Type: Journal Paper (JP)

Treatment: Practical (P); Product Review (R)

Abstract: The test and measurement industry has already embraced DSP for new product concepts as well as for enhancing the capabilities of their existing product offering. A block diagram of a typical DSP based system is shown. The TriStar single-chip programmable digital signal processor uses a Harvard architecture, prefetched instructions, wide instruction word, two external data memories, and extensive parallelism to provide high performance and throughput in waveform processing. Although its architecture has been optimised for test instruments, the TriStar is capable of performing general digital signal **processing** tasks. The **block** diagram of the processor is shown. The chip includes a 16*32 bit three-**port** data register **file**, four 16*20 bit address register files, and a 16*20 bit instruction address stack. These elements are **organised** to **form** three major **units**: an arithmetic **unit** (AU), an address computation **unit** (ACU), and an instruction fetch **unit** (IFU), which all **operate** in parallel. The TriStar is a single cycle machine with all instructions executed in 150 nsec cycle time. The two Data memories and the instruction memory are separated to allow for simultaneous fetching of instructions and accessing of data. Communications between the units is via status flags and a register Bus. The AU internal data path is 32 bits wide allowing execution of many double precision (32 bit) operations. (0 Refs)

Subfile: B C

24/7/3 (Item 2 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2006 Institution of Electrical Engineers. All rts. reserv.

03586819 INSPEC Abstract Number: C86010777

Title: A functional mapping for microprocessor system simulation

Author(s): Marshall, W.K.; Zobrist, G.W.; Bach, W.; Richardson, A.

Author Affiliation: Graduate Eng. Center, Missouri Univ., Rolla, MO, USA

Conference Title: 1985 IEEE Microprocessor Forum (Design Productivity Through Engineering Workstations) (Cat. No. 85CH2151-9) p.15-19

Publisher: IEEE Comput. Soc. Press, Silver Spring, MD, USA

Publication Date: 1985 Country of Publication: USA x+181 pp.

ISBN: 0 8186 0616 9

U.S. Copyright Clearance Center Code: CH2151-9/85/0000-0015\$01.00

Conference Sponsor: IEEE

Conference Date: 2-4 April 1985 Conference Location: Atlantic City, NJ, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: The object **code portion** of a microprocessor must be modeled in order to functionally simulate a microprocessor-based electronic **system**. The automated technique presented here for creating functionally equivalent high-level **programs** for the executable **portion** of the **software represents one step** towards the total automation of the simulation **model building process**. The **block** primitives provide a convenient way to simulate **sections** of the microcode rather than individual statements. The instruction timing preserved for each block can be incorporated into the simulation in order to maintain timing resolution with respect to other simulation models. The table-lookup-driven translation scheme makes switching possible between a variety of simulation languages with minimal changes to the translator software. (6 Refs)

Subfile: C

24/7/4 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC
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02319529 INSPEC Abstract Number: C79009900

**Title: Closing the software gap for interactive mini/microcomputation:
direct execution of microprogrammed block-diagram primitives**

Author(s): Korn, G.A.

Author Affiliation: Univ. of Arizona, Tucson, AZ, USA

Conference Title: Proceedings of COMPSAC 78 Computer Software and
Applications Conference p.93-103

Publisher: IEEE, New York, NY, USA

Publication Date: 1978 Country of Publication: USA xiv+832 pp.

Conference Sponsor: IEEE

Conference Date: 13-16 Nov. 1978 Conference Location: Chicago, IL, USA

Language: English Document Type: Conference Paper (PA)

Treatment: General, Review (G)

Abstract: Block-diagram programs, for instrumentation, control, and simulation systems are especially easy to translate, since no explicit precedence analysis is needed. Block-diagram primitives range from simple adders to complete real-time controllers. They are pure-procedure, reentrant microprograms or threaded code in read-only memory, which may be pre-programmed and plugged in for special applications. In addition to hand 'assembly' and optimizing compilation of the block-diagram programs, the author exhibits the direct-executive MICRODARE II system, which embeds block-diagram 'assembly' in an advanced BASIC dialect serving for interactive editing, job control, and file manipulation. Execution speeds of the systems permit LSI 11 microcomputers and PDP 11 minis to match and exceed those of a CDC 6400; a number of examples are shown. The report continues with a discussion of future multi-task, multiprocessor real-time BASIC **systems** incorporating MICRODARE. The author finally **describes** a new two-processor **system** consisting of an LSI-11 running MICRODARE **software** joined by a two- **port** memory to an ultra-fast bit-sliced 2903/2910 **processor** executing **block** -diagram microprograms. (13 Refs)

Subfile: C

24/7/5 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS
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0687226 NTIS Accession Number: FE-2275-4/XAB

**Systems Studies of Coal Conversion Processes Using a Reference Simulator.
Quarterly Report, April 1, 1977--June 30, 1977**

Reklaitis, G. V. ; Woods, J. M. ; Kayihan, F. ; Sood, M.

Purdue Univ., Lafayette, Ind.

Corp. Source Codes: 5347000

Sponsor: Department of Energy.

Jul 77 41p

Journal Announcement: GRAI7812; NSA0300

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NTIS Prices: PC A03/MF A01

Contract No.: EX-76-C-01-2275

Preliminary user's manuals were prepared for the physical properties code package and for the **process** block material balancing code. These codes together with a major portion of the process equipment calculation **system** were released to ORNL, Lehigh University, and ERDA-Aberdeen. Significant process has been made in the pyrolysis section model and on the process equipment calculation **system**. Manuals for these codes are under preparation. The equipment **calculation system** has been linked with the properties package and expansion of the **module** library is **proceeding**. Development work has continued on the equipment costing **system** and the hydrotreating models. The cost data files have been implemented on the computer and work is in **progress** on the file manipulation and costing **subroutines**. Literature review is complete on the hydrotreating **section** and semi-empirical **model** equations have been assembled and fitted to available data. Further flowsheet modelling will be suspended until a base case flowsheet is developed. (ERA citation 03:013635)

25/6/1 (Item 1 from file: 8)
06620911
Title: Proceedings of the IEEE 2003 Custom Integrated Circuits Conference
Conference Title: Proceedings of the IEEE 2003 Custom Integrated Circuits Conference
Publication Year: 2003

25/6/2 (Item 2 from file: 8)
06512808
Title: Implementation of reconfigurable transceiver based on digital if for multiple wideband CDMA signals
Conference Title: 57th IEEE Semiannual Vehicular Technology Conference (VTC2003)
Publication Year: 2003

25/6/3 (Item 3 from file: 8)
06395060
Title: Low power very large scale integration prototype for three-dimensional discrete wavelet transform processor with medical applications
Publication Year: 2003

25/6/4 (Item 4 from file: 8)
06383239
Title: Variable-rate space-time block codes in M-ary PSK systems
Publication Year: 2003

25/6/5 (Item 5 from file: 8)
05327627
Title: Mini-angle measurement using CCD and laser-collimation
Publication Year: 1998

25/6/6 (Item 6 from file: 8)
04702166
Title: Detection of implicit parallelisms in the task parallel language
Conference Title: Proceedings of the 1997 2nd High Performance Computing on the Information Superhighway, HPC Asia'97
Publication Year: 1997

25/6/7 (Item 7 from file: 8)
04142218
Title: Efficient convolution without input-output delay
Publication Year: 1995

25/6/8 (Item 1 from file: 35)
01222509 ORDER NO: AAD92-16466
HIGH PERFORMANCE ADAPTIVE AND NON-ADAPTIVE DIGITAL SIGNAL PROCESSORS
Year: 1992

25/6/9 (Item 2 from file: 35)
01209642 ORDER NO: AAD92-09040
ON A MULTI-BLOCK METHOD FOR TRANSONIC TURBULENT FLOWS PAST A WING-FUSELAGE CONFIGURATION

Year: 1991

25/6/10 (Item 1 from file: 2)
09203690 INSPEC Abstract Number: C2005-01-1340E-015
Title: Real-time single neuron adaptive control system based on Matlab environment
Publication Date: 2004
Copyright 2004, IEE

25/6/11 (Item 2 from file: 2)
09106562 INSPEC Abstract Number: B2004-10-6250-472
Title: Implementation of reconfigurable transceiver based on digital IF for multiple wideband CDMA signals
Publication Date: 2003
Copyright 2004, IEE

25/6/12 (Item 3 from file: 2)
08624590 INSPEC Abstract Number: C2003-06-7445-021
Title: A hardware/software co-design method in development of ITS information processing and control system
Publication Date: Dec. 2002
Copyright 2003, IEE

25/6/13 (Item 4 from file: 2)
08589998 INSPEC Abstract Number: A2003-10-8760I-041, B2003-05-7510N-088, C2003-05-7330-424
Title: Low power very large scale integration prototype for three-dimensional discrete wavelet transform processor with medical applications
Publication Date: April 2003
Copyright 2003, IEE

25/6/14 (Item 5 from file: 2)
08067989 INSPEC Abstract Number: C2001-11-7420D-007
Title: A Matlab to VHDL conversion toolbox for digital control
Publication Date: 2001
Copyright 2001, IEE

25/6/15 (Item 6 from file: 2)
06885406 INSPEC Abstract Number: B9805-6140C-479, C9805-5260B-247
Title: A mesh-interpolation scheme for very-low bitrate coding of video sequences
Publication Date: Jan.-Feb. 1998
Copyright 1998, IEE

25/6/16 (Item 7 from file: 2)
06723228 INSPEC Abstract Number: A9722-0130C-066, B9711-0100-093, C9711-5260-088
Title: 1997 IEEE International Conference on Acoustics, Speech, and Signal Processing
Publication Date: 1997
Copyright 1997, IEE

25/6/17 (Item 8 from file: 2)
06577962 INSPEC Abstract Number: C9706-6150C-023
Title: Detection of implicit parallelisms in the task parallel language
Publication Date: 1997
Copyright 1997, IEE

25/6/18 (Item 9 from file: 2)
05618590 INSPEC Abstract Number: B9404-7220-008, C9404-5260-040
Title: The PRISM 2.2 real time signal processing system
Publication Date: 1992

25/6/19 (Item 10 from file: 2)
04305055 INSPEC Abstract Number: C89013656
Title: A cache controller for multiprocessing
Publication Date: 1988

25/6/20 (Item 1 from file: 94)
05313412 JICST ACCESSION NUMBER: 03A0026664 FILE SEGMENT: JICST-E
A Hardware/Software Co-design Method in Development of ITS Information
Processing and Control System., 2002

25/6/21 (Item 1 from file: 144)
17216308 PASCAL No.: 05-0287873
Motion analysis in 3D DCT domain and its application to video coding
2005

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25/6/22 (Item 2 from file: 144)
16574457 PASCAL No.: 04-0223265
Implementation of digital transceiver for multiple CDMA signals
HSNMC 2003 : high-speed networks and multimedia communications : Estoril,
23-25 July 2003
2003

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25/6/23 (Item 3 from file: 144)
16090054 PASCAL No.: 03-0247267
Low power very large scale integration prototype for three-dimensional
discrete wavelet transform processor with medical applications
2003

25/6/24 (Item 4 from file: 144)
14626927 PASCAL No.: 00-0297496
Robust coding of images using EBCOT and RVLC
1999 IEEE 3rd workshop on multimedia signal processing : Copenhagen,
13-15 September 1999
1999

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25/6/25 (Item 5 from file: 144)

14491285 PASCAL No.: 00-0153879
Robust image coding with EBCOT and RVLC
Applications of digital image processing XXII : Denver CO, 20-23 July
1999
1999

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25/6/26 (Item 6 from file: 144)
13493718 PASCAL No.: 98-0191383
A mesh-interpolation scheme for very-low bitrate coding of video
sequences
1998

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25/6/27 (Item 1 from file: 34)
11995188 Genuine Article#: BX36Q Number of References: 12
Title: Implementation of digital transceiver for multiple CDMA signals (ABSTRACT AVAILABLE)
Publication date: 20030000

25/6/28 (Item 2 from file: 34)
11591880 Genuine Article#: 670DL Number of References: 17
Title: Low power very large scale integration prototype for three-dimensional discrete wavelet transform processor with medical applications (ABSTRACT AVAILABLE)
Publication date: 20030400

25/6/29 (Item 3 from file: 34)
06506659 Genuine Article#: YX844 Number of References: 10
Title: A mesh-interpolation scheme for very-low bitrate coding of video sequences (ABSTRACT AVAILABLE)
Publication date: 19980100

25/6/30 (Item 4 from file: 34)
02813589 Genuine Article#: MF640 Number of References: 5
Title: CHALLENGES IN MODELING THE RDH PROCESS - A DISCONTINUOUS DYNAMIC SYSTEM (Abstract Available)

25/6/31 (Item 1 from file: 99)
1186253 H.W. WILSON RECORD NUMBER: BAST94054885
Two-dimensional block diagonal LMS adaptive filtering
19940900

25/6/32 (Item 2 from file: 99)
1133224 H.W. WILSON RECORD NUMBER: BAST94001769
Challenges in modeling the RDH process: a discontinuous dynamic system
19931100

25/6/33 (Item 1 from file: 95)
00836320 E94090567357
Speech technology lets machines do the talking

(Sprachsynthesetechnologie fuer Computer)
1994

25/6/34 (Item 1 from file: 62)

20030400

01041065

Low power very large scale integration prototype for three-dimensional
discrete wavelet transform processor with medical applications

27/7/1 (Item 1 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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07031765 E.I. No: EIP04398372079

Title: Virtual memory window for application-specific reconfigurable coprocessors

Author: Vuletic, Miljan; Pozzi, Laura; Ienne, Paolo
Corporate Source: Processor Architecture Laboratory Swiss Fed. Inst. Technol. Lausanne EPFL I and C LAP, 1015 Lausanne, Switzerland
Conference Title: Proceedings of the 41st Design Automation Conference
Conference Location: San Diego, CA, United States Conference Date: 20040607-20040611

Sponsor: Association for Computing Machinery (ACM/SIGDA); Electronic Design Automation, EDA Consortium; Institute of Electrical and Electronics Engineers, IEEE; IEEE Circuits and Systems Society, CASS/CANDE; IEEE Solid State Circuits Society, SSSC

E.I. Conference No.: 63484

Source: Proceedings - Design Automation Conference Proceedings of the 41st Design Automation Conference 2004. (IEEE cat n 04CH37531)

Publication Year: 2004

CODEN: PDAWDJ ISSN: 0738-100X

Language: English

Document Type: CA; (Conference Article) Treatment: A; (Applications); T; (Theoretical)

Journal Announcement: 0409W5

Abstract: Reconfigurable Systems-on-Chip (SoCs) on the market consist of full-fledged processors and large Field-Programmable Gate-Arrays (FPGAs). The latter can be used to implement the system glue logic, various peripherals, and application-specific coprocessors. Using FPGAs for application-specific coprocessors has certain speedup potentials, but it is less present in practice because of the complexity of interfacing the software application with the coprocessor. Another obstacle is the lack of portability across different systems. In this work, we present a virtualisation layer consisting of an operating-system extension and a hardware component. It lowers the complexity of interfacing and increases portability potentials, while it also allows the coprocessor to access the user virtual memory through a virtual memory window. The burden of moving data between processor and coprocessor is shifted from the programmer to the operating system. Since the **virtualisation** layer components hide physical details of the system, user designed hardware and software become perfectly portable. A reconfigurable SoC running Linux is used to prove the viability of the concept. Two **applications** are **ported** to the system for testing the approach, with their critical functions mapped to the specific coprocessors. We show a significant speedup compared to the software versions, while limited penalty is paid for **virtualisation**. 17 Refs.

27/7/2 (Item 2 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
(c) 2006 Elsevier Eng. Info. Inc. All rts. reserv.

03094169 E.I. Monthly No: EIM9107-033708

Title: Porting an iterative parallel region growing algorithm from the MPP to the MasPar MP-1.

Author: Tilton, James C.

Corporate Source: NASA Goddard Space Flight Center, Greenbelt, MD, USA

Conference Title: Proceedings of the 3rd Symposium on the Frontiers of Massively Parallel Computation - Frontiers '90

Conference Location: College Park, MD, USA Conference Date: 19901008

Sponsor: IEEE Computer Soc; IEEE Natl Capital Area Council; NASA; Univ of Maryland

E.I. Conference No.: 14589

Source: Proc 3 Symp Front Massively Parallel Comput Frontiers 90. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA (IEEE cat n 90CH2908-2). p 170-173

Publication Year: 1990

ISBN: 0-8186-2053-6

Language: English

Document Type: PA; (Conference Paper) Treatment: A; (Applications)

Journal Announcement: 9107

Abstract: An iterative parallel region growing (IPRG) algorithm, developed and implemented on the massively parallel processor (MPP) at NASA Goddard, is described. The experience of porting the IPRG algorithm from the MPP to the MasPar MP-1 is related. Porting was very easy and straightforward, especially when Dorband's **virtualization software** was used. The **porting** discussed here, consisting of 1879 lines of MPL code, was accomplished in just two weeks by the author. The major difference between the two implementations is that the looping over virtual parallel arrays had to be done explicitly and had to be the outermost loop (for efficiency) in the MPP Pascal implementation, whereas the same looping was done implicitly in the MPL implementation and could be done in the innermost loop. In a performance test on a 256 multiplied by 256 pixel section of a seven-band Landsat Thematic Mapper image data set, the smaller MasPar MP-1 computer had roughly the same or better performance as the MPP. In the initial iterations, when the regions were still very small, the MPP was about 25% faster than the MasPar MP-1. By iteration 14, the MasPar MP-1 was 33% faster than the MPP, and for ensuing iterations indications are that the MasPar MP-1 speedup versus the MPP will be even larger. 6 Refs.

27/7/3 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online
(c) 2006 ProQuest Info&Learning. All rts. reserv.

01847286 ORDER NO: AADAA-I3023885

Virtualizing operating systems for distributed services on networked workstations

Author: Boyd, Thomas Alford, III

Degree: Ph.D.

Year: 2001

Corporate Source/Institution: Arizona State University (0010)

Chair: Partha Dasgupta

Source: VOLUME 62/08-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 3684. 178 PAGES

ISBN: 0-493-35687-8

Computer applications and operating systems can be augmented with additional functionality by injecting binary code into the boundary layer between them, without tampering with their binaries or recompiling their source. Using this and replaced with virtual bindings. This scheme is called "virtualization." This research designs and prototypes a virtualizing Operating System (vOS), residing on top of Windows 2000, which injects and manages common off-the-shelf applications with virtualizing software. The vOS makes it possible to build cooperative communities of systems that execute applications and share resources completely non-intrusively, while retaining full application binary compatibility.

This research describes a system that manages the virtualization of the Windows 2000 system resources and applications intercepting Application Programming Interface (API) calls. New functionality and mobility are added to the virtualized resources and applications without their knowledge or involvement. This research also extends our prior results of techniques to perform basic application or process migration with active network connections.

The result of our research is the architecture and implementation of a system that supports **virtualization** and migration. Several unique solutions were developed in this research, which demonstrates how to migrate general-purpose applications. This research is part of a larger project called Computing Communities (CC) which is building large unions of distributed machines supporting shared resource management for legacy **applications**.

A **portion** of this research demonstrates how to virtualize an application's Graphic User Interface (GUI) window, making it possible to relocate the window to a remote machine without the application's awareness of the relocation. Thus a common application's window is replicated, or cloned, onto a display on a remote machine. Then, utilizing API interception principles, the application semantics are applied to the clone window by message flow connection to the original application and control data flow.

27/7/4 (Item 2 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online
(c) 2006 ProQuest Info&Learning. All rts. reserv.

01536163 ORDER NO: AAD97-09942

**DESIGNING VIRTUAL MEMORY SYSTEMS FOR PARALLEL AND DISTRIBUTED COMPUTING
(PARALLEL COMPUTING)**

Author: REIS, VERONICA LAGRANGE MOUTINHO DOS

Degree: PH.D.

Year: 1996

Corporate Source/Institution: UNIVERSITY OF CALIFORNIA, IRVINE (0030)

Chair: ISAAC D. SCHERSON

Source: VOLUME 57/10-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 6374. 121 PAGES

Modern parallel machines, such as the CRAY T3D, do not provide virtual memory: it is the programmer's responsibility to adapt the data to the physical memory available or to code any required out-of-core space. However, virtual memory is an important feature in terms of programming convenience, code portability and in providing time-shared environments. Because different machines have different physical memory sizes, **virtualization** allows **programs** to be **ported** across machines without the need to redefine data structures and eventually having to add out-of-core code. Virtual memory also provides a more flexible platform for time-sharing once the real amount of physical memory given to a program may change over time.

Starting from an analysis of the current state of the art and previous attempts to implement parallel virtual memory systems, this dissertation analyzes the issues involved and demonstrates why parallel virtual memory is not straightforward from sequential virtual memory. Once the issues are presented, a model and two policies to implement parallel virtual memory are proposed. These policies, called static and dynamic are extensively analyzed and experimented with, through simulations, for different parallel environments: a tightly coupled massively parallel processor (MPP) and a loosely coupled network of workstations.

Results collected indicate the feasibility and low cost of providing parallel virtual memory. Between the policies proposed, however, it is not clear which one would provide better performance in any environment. This is the case because the different policies presented conflicting results under different environments. For example, in the single user case, the dynamic policy is a marginally better choice for an MPP while the static policy is a clearly better choice for a network of workstations. For the time-shared environments simulated, on the other hand, dynamic policy presented a better performance in nearly all cases (for both an MPP and a network of workstations).

27/7/5 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
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09184150

Title: Breaking news and server gridlock

Author(s): Higgins, K.J.

Journal: Network Computing vol.14, no.23 p.111-16

Publisher: CMP Media Inc,

Publication Date: 13 Nov. 2003 Country of Publication: USA

CODEN: NETCF7 ISSN: 1046-4468

SICI: 1046-4468(20031113)14:23L:111:BNSG;1-E

Material Identity Number: H327-2003-023

Language: English Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: MediaNews Group Interactive's Web servers were taking as long as 50 seconds to render a page during peak periods, and sometimes the sessions crashed altogether. The sluggish Web site was turning off readers, which put the publishing company at risk of losing advertisers, too. MNG Interactive traced the problem to a content management application: the software didn't recognize MNG's vanity URLs, so the Web server was punting all URL requests to the back-end application servers. MediaNews installed Redline's appliance, primarily to translate the URLs, which gave the app servers a rest. The new device also manages all inbound client connections, and its compression feature helped cut download times nearly in half for many of MNG's sites. It also saved the company about \$5,000 a month in extra bandwidth costs. The publishing company will upgrade to version 7.0 of Vignette for managing, but not delivering, content. MediaNews also won't scrap its existing server architecture with the new **portal**. The new **software** will run on the Windows 2000 or Windows 2000 Advanced Server platforms. The publishing company has upgraded its storage area network from 1GB to 2GB of storage and added storage **virtualization** software from Fujitsu to increase its I/O throughput and provide better management of its storage.

Subfile: D

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27/7/6 (Item 2 from file: 2)

DIALOG(R)File 2:INSPEC

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09152347 INSPEC Abstract Number: B2004-12-1265F-019, C2004-12-7410D-072

Title: Virtual memory window for application-specific reconfigurable coprocessors

Author(s): Vuletic, M.; Pozzi, L.; Lenne, P.

Author Affiliation: Processor Archit. Lab., Swiss Fed. Inst. of Technol., Lausanne, Switzerland

Conference Title: Proceedings 2004. Design Automation Conference (IEEE Cat. No.04CH37531) p.948-53

Publisher: ACM, New York, NY, USA

Publication Date: 2004 Country of Publication: USA xxxv+969 pp.

ISBN: 1 58113 828 8 Material Identity Number: XX-2004-01477

U.S. Copyright Clearance Center Code: 1 58113 828 8/2004/0006...\$5.00

Conference Title: Proceedings 2004. Design Automation Conference

Conference Sponsor: ACM; SIGDA; EDA Consortium; IEEE CASS/CANDE

Conference Date: 7-11 June 2004 Conference Location: San Diego, CA, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Applications (A); Practical (P)

Abstract: Reconfigurable systems-on-chip (SoCs) on the market consist of full-fledged processors and large field-programmable gate-arrays (FPGAs). The latter can be used to implement the system glue logic, various peripherals, and application-specific coprocessors. Using FPGAs for application-specific coprocessors has certain speedup potentials, but it is less present in practice because of the complexity of interfacing the software application with the coprocessor. Another obstacle is the lack of portability across different systems. We present a virtualisation layer consisting of an operating-system extension and a hardware component. It lowers the complexity of interfacing and increases portability potentials, while it also allows the coprocessor to access the user virtual memory through a virtual memory window. The burden of moving data between processor and coprocessor is shifted from the programmer to the operating system. Since the **virtualisation** layer components hide physical details of the system, user designed hardware and software become perfectly portable. A reconfigurable SoC running Linux is used to prove the viability of the concept. Two **applications** are **ported** to the system for testing the approach, with their critical functions mapped to the specific coprocessors. We show a significant speedup compared to the software versions, while limited penalty is paid for **virtualisation**. (17 Refs)

Subfile: B C

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27/7/7 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

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06161056 INSPEC Abstract Number: B9602-6210R-057, C9602-6130M-052

Title: Interactive multimedia communications experiment with a networked CD-i prototype

Author(s): Dixon, J.L.; Gelman, A.D.; Khandelwal, R.B.; van de Haar, P.G.; Schoenmakers, A.F.; de Lang, D.

Author Affiliation: Bellcore, Morristown, NJ, USA

Conference Title: MULTIMEDIA '94. 5th IEEE COMSOC International Workshop on Multimedia Communications p.8/3/1-5

Publisher: IEEE, New York, NY, USA

Publication Date: 1994 Country of Publication: USA 283 pp.

Material Identity Number: XX94-00805

Conference Title: 5th International Workshop on Multimedia Communications

Conference Sponsor: IEEE Commun. Soc

Conference Date: 16-19 May 1994 Conference Location: Kyoto, Japan

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: Compact Disc-interactive is a platform which matches the bit rate of the ADSL transmission technology and the MPEG video compression algorithm. ADSL technology, coupled with the MPEG video compression algorithm, provides an ideal medium for delivery of video-on-demand and multimedia services over the existing telephone copper based loop plant. The ADSL allows for video delivery with full user control, simultaneous with existing voice services, over a single non loaded twisted pair up to 18kft or 5.5km in length. A working prototype of the complete end to end system including a networked CD-i player is demonstrated and described. The necessary technologies are now here for possible residential multimedia applications. Our experiment demonstrates feasibility of networking of the existing multimedia platforms which were originally designed for CD-ROM based stand alone systems. The approach to **applications porting** by **virtualization** these platforms is advantageous due to the existing popularity of titles as well as the existing application development systems for creation of new applications. (8 Refs)

Subfile: B C

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27/7/8 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC
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04887456 INSPEC Abstract Number: C91036498

Title: Porting an iterative parallel region growing algorithm from the MPP to the MasPar MP-1

Author(s): Tilton, J.C.

Author Affiliation: NASA Goddard Space Flight Center, Greenbelt, MD, USA

Conference Title: Third Symposium on the Frontiers of Massively Parallel Computation. Proceedings. (Cat. No.90CH2908-2) p.170-3

Editor(s): Jaja, J.

Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA

Publication Date: 1990 Country of Publication: USA xiv+531 pp.

ISBN: 0 8186 2053 6

U.S. Copyright Clearance Center Code: CH2908-2/90/0000-0170\$01.00

Conference Sponsor: IEEE; NASA; Univ. Maryland

Conference Date: 8-10 Oct. 1990 Conference Location: College Park, MD, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P); Theoretical (T)

Abstract: An iterative parallel region growing (IPRG) algorithm, developed and implemented on the massively parallel processor (MPP) at NASA Goddard, is described. The experience of porting the IPRG algorithm from the MPP to the MasPar MP-1 is related. Porting was very easy and straightforward, especially when the Dorband **virtualization software** was used. The **porting** discussed, consisting of 1879 lines of MPL code, was accomplished in just two weeks by the author. The major difference between the two implementations is that the looping over virtual parallel arrays had to be done explicitly and had to be the outermost loop (for efficiency) in the MPP Pascal implementation, whereas the same looping was done implicitly in the MPL implementation and could be done in the innermost loop. In a performance test on a 256*256 pixel section of a seven-band Landsat thematic mapper image data set, the smaller MasPar MP-1 computer had roughly the same or better performance as the MPP. In the initial iterations, when the regions were still very small, the MPP was about 25% faster than the MasPar MP-1. By iteration 14, the MasPar MP-1 was 33% faster than the MPP, and for ensuing iterations indications are that the MasPar MP-1 speedup versus the MPP will be even larger. (6 Refs)

Subfile: C

27/7/9 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal
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17454660 PASCAL No.: 06-0037045
**Virtual memory window for application-specific reconfigurable
coprocessors**

**Design automation conference : proceedings 2004 : 41st DAC : San Diego
Convention Center, San Diego, CA, June 7-11, 2004**

VULETIC Miljan; POZZI Laura; IENNE Paolo

Swiss Federal Institute of Technology Lausanne Processor Architecture
Laboratory EPFL I&C LAP, IN-F Ecublens, 1015 Lausanne, Switzerland

Association for computing machinery. Special interest group on design
automation, United States

Design automation conference, 41 (San Diego CA USA) 2004-06-07
2004 948-953

Publisher: Association for Computing Machinery, New York NY; IEEE,
Piscataway

ISBN: 1-58113-828-8 Availability: INIST-Y 38555; 354000138664061870

No. of Refs.: 17 ref.

Document Type: C (Conference Proceedings) ; A (Analytic)

Country of Publication: United States

Language: English

Reconfigurable Systems-on-Chip (SoCs) on the market consist of full-fledged processors and large Field-Programmable Gate-Arrays (FPGAs). The latter can be used to implement the system glue logic, various peripherals, and application-specific coprocessors. Using FPGAs for application-specific coprocessors has certain speedup potentials, but it is less present in practice because of the complexity of interfacing the software application with the coprocessor. Another obstacle is the lack of portability across different systems. In this work, we present a virtualisation layer consisting of an operating-system extension and a hardware component. It lowers the complexity of interfacing and increases portability potentials, while it also allows the coprocessor to access the user virtual memory through a virtual memory window. The burden of moving data between, processor and coprocessor is shifted from the programmer to the operating system. Since the **virtualisation** layer components hide physical details of the system, user designed hardware and software become perfectly portable. A reconfigurable SoC running Linux is used to prove the viability of the concept. Two **applications** are **ported** to the system for testing the approach, with their critical functions mapped to the specific coprocessors. We show a significant speedup compared to the software versions, while limited penalty is paid for **virtualisation**.

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27/7/10 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal
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16636273 PASCAL No.: 04-0286717
It's time to turn on that utility

TINHAM B

Journal: Manufacturing Computer Solutions, 2004, 10 (4) 27-29

ISSN: 1358-1066 CODEN: MCSOFD Availability: INIST-XXXX

Document Type: P (Serial) ; A (Analytic)

Country of Publication: United Kingdom

Language: English

The bringing of on-demand by utility computing is discussed, which provides co-operative, distributed, computer-intensive operations. The grid/utility and on-demand not only gathers vast compute power for engineering analysis problems, but also cuts costs by further consolidating IT infrastructures, and also improving utilisation, availability and flexibility. The utility computing programme could be used to configure stuff on the portal, and could also reconfigure large amounts of the system from anywhere in real time. It also got high availability, no single point of failure, full security policy, fibre channel storage networking and dual power grids, and the risk factors around consolidation also goes down with grid, since reconfiguring is quick.

28/6/1 (Item 1 from file: 8)

07407462

Title: Storage virtualized - Finally

Publication Year: 2005

28/6/2 (Item 2 from file: 8)

06922258

Title: Proceedings: Web3D 2004 - 9th international conference on 3D web technology

Conference Title: Proceedings - 9th International Conference on 3D Web Technology

Publication Year: 2004

28/6/3 (Item 3 from file: 8)

05845590

Title: An adaptive parallel system dedicated to projective image matching

Conference Title: International Conference on Image Processing (ICIP 2000)

Publication Year: 2000

28/6/4 (Item 4 from file: 8)

01744763

Title: METHOD FOR PORTABLE COMMUNICATION PROTOCOL PROGRAM.

Publication Year: 1984

28/6/5 (Item 1 from file: 35)

02052074 ORDER NO: AADAA-I3154576

Execution of unmodified applications on distributed storage and compute resources

Year: 2004

28/6/6 (Item 2 from file: 35)

01536163 ORDER NO: AAD97-09942

DESIGNING VIRTUAL MEMORY SYSTEMS FOR PARALLEL AND DISTRIBUTED COMPUTING (PARALLEL COMPUTING)

Year: 1996

28/6/7 (Item 1 from file: 2)

09894413

Title: A modular architecture for hot swappable mobile ad hoc routing algorithms

Publication Date: 2005

Copyright 2006, The Institution of Engineering and Technology

28/6/8 (Item 2 from file: 2)

09438803 INSPEC Abstract Number: C2005-07-7430-004

Title: The architecture of virtual machines

Publication Date: May 2005

Copyright 2005, IEE

28/6/9 (Item 3 from file: 2)

09311628

Title: All change for software costs [software licensing analysis]

Publication Date: 22 Nov. 2004
Copyright 2005, IEE

28/6/10 (Item 4 from file: 2)
08797375 INSPEC Abstract Number: C2004-01-6150J-012
Title: The design and implementation of Zap: a system for migrating computing environments
Publication Date: 2002
Copyright 2003, IEE

28/6/11 (Item 5 from file: 2)
07998652 INSPEC Abstract Number: B2001-09-6135E-113, C2001-09-5260B-374
Title: An adaptive parallel system dedicated to projective image matching
Publication Date: 2000
Copyright 2001, IEE

28/6/12 (Item 6 from file: 2)
07899938 INSPEC Abstract Number: C2001-05-5210B-071
Title: Behavioural language compilation with virtual hardware management
Publication Date: 2000
Copyright 2001, IEE

28/6/13 (Item 7 from file: 2)
07826448 INSPEC Abstract Number: B2001-03-6210L-060, C2001-03-5620L-012
Title: Transparent network connectivity in dynamic cluster environments
Publication Date: 2000
Copyright 2001, IEE

28/6/14 (Item 8 from file: 2)
04666998 INSPEC Abstract Number: B90045690, C90046582
Title: Impact of OSI on the architecture of the design of application processes
Publication Date: 1989

28/6/15 (Item 9 from file: 2)
03176483 INSPEC Abstract Number: B84006591, C84006559
Title: Specification oriented switching program structure
Publication Date: 1983

28/6/16 (Item 10 from file: 2)
02816433 INSPEC Abstract Number: C82013032
Title: CPU virtualization in DIPS virtual machine system
Publication Date: 1981

28/6/17 (Item 1 from file: 144)
17196791 PASCAL No.: 05-0267056
The architecture of virtual machines
2005

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28/6/18 (Item 2 from file: 144)

14825943 PASCAL No.: 00-0508975
Transparent network connectivity in dynamic cluster environments
Network-based parallel computing : communication, architecture, and
applications : toulouse, 8 January 2000
2000

Copyright (c) 2000 INIST-CNRS. All rights reserved.

28/6/19 (Item 3 from file: 144)
14816819 PASCAL No.: 00-0499309
Behavioural language compilation with virtual hardware management
FPL 2000 : field-programmable logic and applications : the roadmap to
reconfigurable computing : Villach, 27-30 August 2000
2000

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28/6/20 (Item 1 from file: 34)
13890179 Genuine Article#: 922KM Number of References: 12
Title: The architecture of virtual machines (ABSTRACT AVAILABLE)
Publication date: 20050500

28/6/21 (Item 2 from file: 34)
10113110 Genuine Article#: BT02T Number of References: 13
Title: Transparent network connectivity in dynamic cluster environments (
ABSTRACT AVAILABLE)
Publication date: 20000000

28/6/22 (Item 1 from file: 99)
1158304 H.W. WILSON RECORD NUMBER: BAST94026889
The virtual reality of switched networks
19940501

28/6/23 (Item 1 from file: 266)
00454552
IDENTIFYING NO.: 0509466 AGENCY CODE: NSF
Collaborative Research: CSR: AES: Virtual Playgrounds: Making Virtual
Distributed Computing Real

28/6/24 (Item 2 from file: 266)
00454551
IDENTIFYING NO.: 0509466 AGENCY CODE: NSF
Collaborative Research: CSR: AES: Virtual Playgrounds: Making Virtual
Distributed Computing Real

28/6/25 (Item 3 from file: 266)
00454548
IDENTIFYING NO.: 0509408 AGENCY CODE: NSF
Collaborative Research:CSR: AES: Virtual Playgrounds: Making Virtual
Distributed Computing Real

28/6/26 (Item 1 from file: 95)
02067842 20060304840

A software architecture for mobile applications and services
(Eine Software-Architektur fuer mobile Anwendungen und Dienste)
2005

28/6/27 (Item 2 from file: 95)
01962538 20050602739
The architecture of virtual machines
2005

28/6/28 (Item 3 from file: 95)
00887057 I95034556259
Titel japanisch
(Virtualisierung erweiterter Halbleiterspeicher als
Hauptspeichererweiterung in Vektor-Superrechnern +++)
(Virtualization of semiconductor extended storage as extended main memory
on vector supercomputers)1994

File 15:ABI/Inform(R) 1971-2006/Jun 20
(c) 2006 ProQuest Info&Learning
File 635:Business Dateline(R) 1985-2006/Jun 20
(c) 2006 ProQuest Info&Learning
File 9:Business & Industry(R) Jul/1994-2006/Jun 19
(c) 2006 The Gale Group
File 810:Business Wire 1986-1999/Feb 28
(c) 1999 Business Wire
File 610:Business Wire 1999-2006/Jun 20
(c) 2006 Business Wire.
File 647:CMP Computer Fulltext 1988-2006/Jul W4
(c) 2006 CMP Media, LLC
File 275:Gale Group Computer DB(TM) 1983-2006/Jun 19
(c) 2006 The Gale Group
File 674:Computer News Fulltext 1989-2006/Jun W2
(c) 2006 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2006/Jun 20
(c) 2006 Dialog
File 98:General Sci Abs 1984-2005/Jan
(c) 2006 The HW Wilson Co.
File 624:McGraw-Hill Publications 1985-2006/Jun 20
(c) 2006 McGraw-Hill Co. Inc
File 621:Gale Group New Prod.Annou.(R) 1985-2006/Jun 20
(c) 2006 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2006/Jun 19
(c) 2006 The Gale Group
File 369:New Scientist 1994-2006/Jun W2
(c) 2006 Reed Business Information Ltd.
File 813:PR Newswire 1987-1999/Apr 30
(c) 1999 PR Newswire Association Inc
File 613:PR Newswire 1999-2006/Jun 20
(c) 2006 PR Newswire Association Inc
File 16:Gale Group PROMT(R) 1990-2006/Jun 19
(c) 2006 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
(c) 1999 The Gale Group
File 370:Science 1996-1999/Jul W3
(c) 1999 AAAS
File 148:Gale Group Trade & Industry DB 1976-2006/Jun 20
(c)2006 The Gale Group
File 553:Wilson Bus. Abs. 1982-2006/Jun
(c) 2006 The HW Wilson Co
File 634:San Jose Mercury Jun 1985-2006/Jun 19
(c) 2006 San Jose Mercury News
File 88:Gale Group Business A.R.T.S. 1976-2006/Jun 12
(c) 2006 The Gale Group

Set	Items	Description
S1	185229	(PORT? ? OR PORTAL OR PORTED OR PORTING) (5N) (SOFTWARE OR PROGRAM? ? OR APPLICATION? ? OR CODE? ? OR GAME? ? OR APPLET? ? OR THREAD? ? OR MULTITHREAD? ? OR MULTI()THREAD? ? OR FILE? ? OR MACRO? ? OR SCRIPT?)
S2	25971	(PORT? ? OR PORTAL OR PORTED OR PORTING) (5N) (APP OR APPS OR BROWSER? OR WEBBROWSER? OR SUBROUTIN? OR SUBPROGRAM? OR OS OR OPERATING()SYSTEM? OR EXECUT?()) (FILE? ? OR CODE? ? OR BYTE? - ?))
S3	201945	S1:S2
S4	5249	PROCESS???(2W)BLOCK? ?
S5	12	S4(50N)S3
S6	9	RD (unique items)

6/3,K/1 (Item 1 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2006 ProQuest Info&Learning. All rts. reserv.

02418086 169181271

Microsoft adds wireless notification services

Fontana, John

Network World v19n36 PP: 30 Sep 9, 2002

ISSN: 0887-7661 JRNL CODE: NWW

WORD COUNT: 564

...ABSTRACT: a foundation for creating notification services for wired and wireless users. With SQL Server 2000 Notification Services, network executives can extend corporate, Web-based and **portal applications** with a mechanism that notifies users when updates have been made to information within those applications, such as price changes in a supply-chain application. The notification service is software with SQL as an engine that can **process blocks** of events and using batch processing match them to user subscription requests for updates. But corporations must develop their own front-end interface and hooks...

6/3,K/2 (Item 2 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2006 ProQuest Info&Learning. All rts. reserv.

01061993 97-11387

Xircom jumps into remote access server market

Trowbridge, Dave

Computer Technology Review v15n6 PP: 4 Jun 1995

ISSN: 0278-9647 JRNL CODE: CTN

WORD COUNT: 383

...TEXT: miniport drivers provide seamless integration with Novell's and Microsoft's NOS remote access software. Additionally, Netaccess Multiport Modem Cards have been designed with COM **port** emulation to support other OS environments.

The product also incorporates Xircom's proprietary modem communications interface, the Xircom Mobile Applications Programming Interface API). XMAPI eliminates UART-based, serial-port, single-character **processing** by using **block** -mode data transfers, shared memory, and large data buffers to increase throughput while reducing system overhead. NOS software drivers are optimized to take full advantage...

6/3,K/3 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2006 CMP Media, LLC. All rts. reserv.

00531390 CMP ACCESSION NUMBER: EET19930927S1677
DSPs MOVING UP TO OBJECT-ORIENTED PROGRAMS
KLAS NILSSON DEPT. OF AUTOMATIC CONTROL LUND INSTITUTE OF TECHNOLOGY
ELECTRONIC ENGINEERING TIMES, 1993, n 765, 76
PUBLICATION DATE: **930927**
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: DSP Part 3: Applications & Technology
WORD COUNT: 1132

... features-operator overloading, conversions, class dependent memory allocation, etc.-are very useful in DSP applications. One approach to simplify DSP programming is to have predefined **processing** software **blocks** that are put together using a graphical programming environment. This is quite attractive, but it is still desirable to have a proper underlying textual representation of the **program**, e.g., in case of **porting** the **software** to other platforms.

Furthermore, most DSP algorithms are naturally expressed by block diagrams, and such blocks are naturally represented by the objects of OOP. Both...

6/3,K/4 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2006 The Gale Group. All rts. reserv.

01294069 SUPPLIER NUMBER: 07149010 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Digital ICs: ISSCC. (integrated circuits, International Solid State
Circuits Conference)

Bursky, Dave
Electronic Design, v37, n4, p49(5)
Feb 23, 1989

ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2827 LINE COUNT: 00211

... MFLOPS.

The processor chip, known as the N10, includes both a 4-kbyte instruction and an 8-kbyte data cache, as well as a five- **port** register **file** for the floating-point subsection. A 64-entry, four-way set-associative translation look-aside buffer is also incorporated in the integer processor's paging logic. The graphics **processor block** performs calculations for hidden-surface removal with a Z-buffer and intensity interpolation. It can generate up to 21 million Gouraud shaded pixels/s with...

6/3,K/5 (Item 2 from file: 275)

DIALOG(R)File 275:Gale Group Computer DB(TM)

(c) 2006 The Gale Group. All rts. reserv.

01213697 SUPPLIER NUMBER: 06015928 (USE FORMAT 7 OR 9 FOR FULL TEXT)

PC-Elevator 386. (Hardware Review) (386 turbo boards) (evaluation)

Marks, Howard

PC Magazine, v6, n18, p245(2)

Oct 27, 1987

DOCUMENT TYPE: evaluation ISSN: 0888-8507 LANGUAGE: ENGLISH

RECORD TYPE: FULLTEXT; ABSTRACT

WORD COUNT: 454 LINE COUNT: 00031

... has to ask your host to get disk data and wait for it to pass it back.

The PC-Elevator 386 talks to the host **processor** through a **block** of dual-port memory and a block of I/O **ports** . This design, combined with the **software** necessary to load software into the 386, prevented the PC-Elevator from running a beta-test version of OS/2. Applied Reasoning says that it...

6/3,K/6 (Item 1 from file: 624)
DIALOG(R)File 624:McGraw-Hill Publications
(c) 2006 McGraw-Hill Co. Inc. All rts. reserv.

00978053

Sea Launch Prepares For Demonstration Mission: Launch rate from the equator could be increased with sufficient demand and additional investment in the system

BRUCE A. SMITH

Aviation Week & Space Technology, Vol. 149, No. 22, Pg 56

November 30, 1998

JOURNAL CODE: AW

SECTION HEADING: SEA LAUNCH DEBUT ISSN: 0005-2175

WORD COUNT: 2,067

TEXT:

...boosters on the ship for each trip to the equator.

Another proposal which has been studied to increase the launch rate is to conduct initial **processing** on the **Block** DM upper stage in a land-based facility at the home port so that it will require less processing time on the ship once the vessel has returned to **port**.

PROGRAM OFFICIALS EARLIER decided to begin operations with a rate of six missions per year, deferring additional up-front program investments in favor of concentrating on...

6/3,K/7 (Item 1 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)
(c) 2006 The Gale Group. All rts. reserv.

01076375 Supplier Number: 40411871 (USE FORMAT 7 FOR FULLTEXT)
EMS ANNOUNCES AN INTEL iAPX 80386 BASED REAL TIME CPU ON THE VMEBUS
News Release, p1
June 8, 1988
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 343

...
serial channels of sync/async communications interface. This supports
both SDLC/HDLC or IBM Bi-sync protocols. The MPSC 8274 is connected
to two RS232 **ports** via the P2 connector.

Software

currently available for the CPU-5RT is the EMS bug-386. This
monitor/debugger software is designed to operate in a Host
development environment or in stand alone mode. Eight basic functions
are provided in two EPROMS installed on the CPU-5RT:

Read and write to memory locations and **processor** registers.

Copy **blocks** of the memory arbitrarily in the memory address

Read and write to I/O **ports**

Execute code - Go and single step

Insert software breakpoints

Disassemble code into xxx86 assembly language mnemonics

Down/upload user programs (standard Intel Hex format)

The monitor can...

6/3,K/8 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2006 The Gale Group. All rts. reserv.

06155285 Supplier Number: 53956276 (USE FORMAT 7 FOR FULLTEXT)
CPU And Memory Advances Propel Chips To New Performance Heights.
Bursky, Dave
Electronic Design, v47, n4, p46(1)
Feb 22, 1999
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 3884

... point sub units and two sets of integer calculations or branch operations, or load/store operations). By clustering the operations, the number of required register- **file ports** and crossbar switches for the data-bus lines can be reduced to roughly one-half that of conventional approaches. This scheme, then, reduces not only the register-file access time, but critical-path delays as well.

Other presentations in the session examined **processing blocks** with an even greater degree of specialization, such as a 32-bit, 64-matrix parallel processor developed by Motorola Inc., Arlington Heights, Ill. The chip...

6/3,K/9 (Item 2 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2006 The Gale Group. All rts. reserv.

03031959 Supplier Number: 44120064 (USE FORMAT 7 FOR FULLTEXT)
DSPs MOVING UP TO OBJECT-ORIENTED PROGRAMS

Electronic Engineering Times, p76

Sept 27, 1993

Language: English Record Type: Fulltext

Document Type: Magazine/Journal; Trade

Word Count: 1126

... features - operator overloading, conversions, class dependent memory allocation, etc. - are very useful in DSP applications. One approach to simplify DSP programming is to have predefined **processing** software **blocks** that are put together using a graphical programming environment. This is quite attractive, but it is still desirable to have a proper underlying textual representation of the **program**, e.g., in case of **porting** the **software** to other platforms.

Furthermore, most DSP algorithms are naturally expressed by block diagrams, and such blocks are naturally represented by the objects of OOP. Both...

?

File 348:EUROPEAN PATENTS 1978-2006/ 200624

(c) 2006 European Patent Office

File 349:PCT FULLTEXT 1979-2006/UB=20060615,UT=20060608

(c) 2006 WIPO/Univentio

Set	Items	Description
S1	20531	(PORT? ? OR PORTAL OR PORTED OR PORTING) (5N) (SOFTWARE OR PROGRAM? ? OR APPLICATION? ? OR CODE? ? OR GAME? ? OR APPLET? ? OR THREAD? ? OR MULTITHREAD? ? OR MULTI()THREAD? ? OR FILE? ? OR MACRO? ? OR SCRIPT?)
S2	1578	(PORT? ? OR PORTAL OR PORTED OR PORTING) (5N) (APP OR APPS OR BROWSER? OR WEBBROWSER? OR SUBROUTIN? OR SUBPROGRAM? OR OS OR OPERATING()SYSTEM? OR EXECUT?() (FILE? ? OR CODE? ? OR BYTE? - ?))
S3	21234	S1:S2
S4	2799599	(SOFTWARE OR PROGRAM? ? OR APPLICATION? ? OR CODE? ? OR GAME? ? OR APPLET? ? OR THREAD? ? OR MULTITHREAD? ? OR MULTI()THREAD? ? OR FILE? ? OR MACRO? ? OR SCRIPT?)
S5	199290	(APP OR APPS OR BROWSER? OR WEBBROWSER? OR SUBROUTIN? OR SUBPROGRAM? OR OS OR OPERATING()SYSTEM? OR EXECUT?() (FILE? ? OR CODE? ? OR BYTE? ?))
S6	580843	S4:S5 (5N) (CONVERT??? OR ADJUST???? OR CHANG??? OR ADAPT? OR CONVERSION? OR ALTER??? OR MODIFY??? OR TRANSLAT? OR TRANSFORM? OR MODIFICATION? ?)
S7	35567	DATASTRUCTUR??? OR DATA()STRUCTUR???
S8	22479	PROCESS??? (2W) BLOCK? ?
S9	392	S7 (50N) S8
S10	0	S3 (30N) S9
S11	16	S6 (30N) S9
S12	44	S3 (30N) S8
S13	534	S6 (30N) S8
S14	8103	S8 (50N) (S4:S5)

11/6,K/1 (Item 1 from file: 348)

DIALOG(R)File 348:(c) 2006 European Patent Office. All rts. reserv.

02059858

Systems and methods for secure transaction management and electronic rights protection

System und Verfahren fur sichere Transaktionsverwaltung und elektronischen Rechteschutz

Systemes et procedes de gestion de transactions securisees et de protection des droits electroniques

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200622	302
SPEC A	(English)	200622	193789
Total word count - document A			194091
Total word count - document B			0
Total word count - documents A + B			194091

...SPECIFICATION may hit limitations of a single threaded device in certain circumstances.

It is preferable when these limitations are unacceptable to use a full "multi-threaded" **data structure** write capabilities. For example, a type of "two-phase commit" processing of the type used by database vendors may be used to allow **data structure** sharing between processes. To implement this "two-phase commit" **process**, each swap **block** may contain page addresses for additional memory blocks that will be used to store **changed** information. A change page is a local copy of a piece of a data element that has been written by an SPE process. The changed page(s) references associated with a specific **data structure** are stored locally to the swap block in the preferred embodiment.

For example, SPE 503 may support two (change pages) per data structure. This limit...

11/6,K/2 (Item 2 from file: 348)

DIALOG(R)File 348:(c) 2006 European Patent Office. All rts. reserv.

02018194

Secure transaction management

Gesicherte Transaktionsverwaltung

Gestion de transactions securisees

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200605	249
SPEC A	(English)	200605	180527
Total word count - document A			180776
Total word count - document B			0
Total word count - documents A + B			180776

...SPECIFICATION may hit limitations of a single threaded device in certain circumstances.

It is preferable when these limitations are unacceptable to use a full "multi-threaded" **data structure** write capabilities. For example, a type of "two-phase commit" processing of the type used by database vendors may be used to allow **data structure** sharing between processes. To implement this "two-phase commit" **process**, each swap **block** may contain page addresses for additional memory blocks that will be used to store changed information. A change page is a local copy of a piece of a data element that has been written by an SPE process. The changed page(s) references associated with a specific **data structure** are stored locally to the swap block in the preferred embodiment.

For example, SPE 503 may support two (**change** pages) per data structure. This limit is easily alterable by changing the size of the swap block structure and allowing the update algorithm to process...

11/6,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:(c) 2006 European Patent Office. All rts. reserv.

01930027

Secure transaction management

Verfahren und Vorrichtung zur gesicherten Transaktionsverwaltung

Procede et dispositif de gestion de transactions securisees

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200529	1002
SPEC A	(English)	200529	194028
Total word count - document A			195030
Total word count - document B			0
Total word count - documents A + B			195030

...SPECIFICATION may hit limitations of a single threaded device in certain circumstances.

It is preferable when these limitations are unacceptable to use a full "multi-threaded" **data structure** write capabilities. For example, a type of "two-phase commit" processing of the type used by database vendors may be used to allow **data structure** sharing between processes. To implement this "two-phase commit" **process**, each swap **block** may contain page addresses for additional memory blocks that will be used to store changed information. A change page is a local copy of a piece of a data element that has been written by an SPE process. The **changed** page(s) references associated with a specific **data structure** are stored locally to the swap block in the preferred embodiment.

For example, SPE 503 may support two (change pages) per data structure. This limit...

11/6,K/4 (Item 4 from file: 348)

DIALOG(R)File 348:(c) 2006 European Patent Office. All rts. reserv.

01908130

Image processing system and image processing method

Bildverarbeitungssystem und Bildverarbeitungsverfahren

Systeme de traitement d'image et procede de traitement d'image

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
----------------	----------	--------	------------

CLAIMS A	(English)	200523	1362
----------	-----------	--------	------

SPEC A	(English)	200523	9632
--------	-----------	--------	------

Total word count - document A	10996
-------------------------------	-------

Total word count - document B	0
-------------------------------	---

Total word count - documents A + B	10996
------------------------------------	-------

...SPECIFICATION the vectors grouped as the closed graphic in step S711 are detected and are grouped as one graphic element (step S712).

With the above-mentioned **process** , a graphic **block** can be handled as an independently re-usable graphic object.

(**Conversion** Process into **Application** Data)

Fig. 12 is a view showing the **data structure** of a file in an intermediate data format obtained as the conversion result of the block selection process (step S1201) and vectorization process (step S1206) for ...

11/6,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:(c) 2006 European Patent Office. All rts. reserv.

01194095

Instruction execution mechanism

Mechanismus zur Befehlsausführung

Mecanisme d'execution d'instructions

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200039	808
SPEC A	(English)	200039	2764
Total word count - document A			3572
Total word count - document B			0
Total word count - documents A + B			3572

...SPECIFICATION block.egress.BLK and
current(underscore)block.egress.BLK->BACS are planted as literal
values, and hence do not require access to the egress **data structure** .

If all the tests in the block-following code are successful, a jump
will be made to the **translated code** for the successor block without
having to call the block completion **process** . Otherwise, the **block**
completion process 20 will be called.

As mentioned above, each **translated target code** block 17 has two
entry points: a first entry point which is used when entry is made from
the block completion process 20, and a...

11/6,K/6 (Item 6 from file: 348)
DIALOG(R)File 348:(c) 2006 European Patent Office. All rts. reserv.

00879062

Memory management system and method for processor having separate code and data contexts

Speicherverwaltungssystem und Verfahren für Prozessor mit getrennten Code- und Datenkontexten

Système et procédé de gestion de mémoire pour processeur avec des contextes de code et de données séparés

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9710W5	723
SPEC A	(English)	9710W5	4571
Total word count - document A			5294
Total word count - document B			0
Total word count - documents A + B			5294

...SPECIFICATION the system determines which translation look-aside buffer (TLB), i.e., code translation look-aside buffer (CTLB) or data translation look-aside buffer generated the **translation** miss fault. If the **code translation** look-aside buffer did not have an entry including the current context identifier and the current virtual address then the **process** flows to **block** 906 where the system scans kernel translation **data structures** for an entry containing both the current virtual address and the current context identifier. The system then, at block 908, retrieves the translation entry including...

11/6,K/7 (Item 7 from file: 348)
DIALOG(R)File 348:(c) 2006 European Patent Office. All rts. reserv.

00738664

A method for programming a data processing system

Verfahren zur Programmierung eines Datenverarbeitungssystems

Methode pour programmer un systeme de traitement de donnees

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	266
SPEC A	(English)	EPAB96	12740
Total word count - document A			13006
Total word count - document B			0
Total word count - documents A + B			13006

...SPECIFICATION both read from external files located in memory 9 or a memory (not shown) in emulation system 15. This data is used to create internal **data structures** used by the Rule Checker and interactive memory mapper software **programs** to allow a user to **modify** a model of data processor to be programmed.

Block 300 is a **process** user actions **block** . During the execution of block 300, the user configures the model of the data processor to be programmed by the Rule Checker and interactive memory...

11/6,K/8 (Item 8 from file: 348)
DIALOG(R)File 348:(c) 2006 European Patent Office. All rts. reserv.

00551327

Method and apparatus for managing class information.

Verfahren und Gerat fur Klasseninformationsverwaltung.

Methode et appareil pour gerer l'information de classe.

LANGUAGE (Publication,Procedural,Application):: English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	570
SPEC A	(English)	EPABF1	3120
Total word count - document A			3690
Total word count - document B			0
Total word count - documents A + B			3690

...SPECIFICATION data structure 54 is made for class information corresponding to the request. Next, block 76 illustrates a determination of whether a search of the class **data structure** resulted in class information corresponding to the request.

If no class data information corresponding to the request is found in the search of the class **data structure**, as determined in block 76, then the **process** passes to **block 78** which illustrates **translating** the request into **application program** interface calls or some other call specific to the graphic user interface operating system and block 80 depicts sending the request to a GUI operating...

11/6,K/9 (Item 9 from file: 348)
DIALOG(R)File 348:(c) 2006 European Patent Office. All rts. reserv.

00306062

Digital data processing system.

Digitales Datenverarbeitungssystem.

Systeme du traitement de donnees numeriques.

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	1018
CLAIMS B	(German)	EPBBF1	868
CLAIMS B	(French)	EPBBF1	1115
SPEC B	(English)	EPBBF1	154256
Total word count - document A			0
Total word count - document B			157257
Total word count - documents A + B			157257

...SPECIFICATION protection cache, and address translation unit;

Fig. 241 is a detailed block diagram of portions of computer system instruction and microinstruction control logic;

Fig. 242 is a detailed **block** diagram of portions of computer system microinstruction control logic;

Fig. 243 is a detailed block diagram of further portions of computer system microinstruction control logic...

11/6,K/10 (Item 10 from file: 348)
DIALOG(R)File 348:(c) 2006 European Patent Office. All rts. reserv.

00273279

Inter-process signal handling in a multi-processor system.

Inter-Prozesssignalverarbeitung in einem Multiprozessorsystem.

Traitement de signaux interprocessus dans un systeme multiprocesseur.

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	966
SPEC A	(English)	EPABF1	3985
Total word count - document A			4951
Total word count - document B			0
Total word count - documents A + B			4951

...SPECIFICATION can be found in the aforementioned Bishop reference.

Detailed Description

The solution, as discussed above, to the problems of multi-processing, can be implemented by **modifying** the basic UNIX **operating system** as detailed below.

The following are additions or modifications to the **process control block** which, as discussed above, is the basic process **data structure** used within the UNIX operating system.

p...

11/6,K/11 (Item 1 from file: 349)
DIALOG(R)File 349:(c) 2006 WIPO/Univentio. All rts. reserv.

01313061 **Image available**
METHOD FOR AT LEAST PARTIALLY COMPENSATING FOR ERRORS IN INK DOT PLACEMENT
DUE TO ERRONEOUS ROTATIONAL DISPLACEMENT
PROCEDE POUR LA COMPENSATION AU MOINS PARTIELLE D'ERREURS DANS LE PLACEMENT
POINTS D'ENCRE DUES A UN DEPLACEMENT ROTATIONNEL ERRONE

Publication Language: English

Filing Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 618378

Publication Year: 2005

Fulltext Availability:

Claims

Claim

... the speed of the RIP, and the amount of memory remaining in SoPEC while printing the previous band(s). Figure 10 shows the high level **data structure** of a number of pages with different numbers of bands in the page. Each compressed band contains a mandatory band header, an optional bi-level plane, optional sets of interleaved contone planes, and an optional tag data plane (for Netpage enabled **applications**). Since each of these planes is optional, the band header specifies which planes are included with the band. Figure 1 1 gives a high-level...

11/6,K/12 (Item 2 from file: 349)
DIALOG(R)File 349:(c) 2006 WIPO/Univentio. All rts. reserv.

00469797 **Image available**
METHOD FOR COMPILING HIGH LEVEL PROGRAMMING LANGUAGES
PROCEDE DE COMPILATION DE LANGAGES DE PROGRAMMATION AVANCEE
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 7037
Publication Year: 1999

Fulltext Availability:
Claims

Claim

... specific circuit is not exceeded.

32 The method of Claim 29, wherein scheduling further comprises:
modeling each group as a separate task;
modeling as a **processor** each available **block** of reconfigurable logic
on an
application specific integrated circuit; and
running a modified multiprocessor scheduling algorithm.

33 The method of Claim 32, wherein the intermediate **data structure** is
a
graph in which arcs represent dependencies, and wherein modeling each
group as a
separate task comprises:
for each group, adding a node to the graph;
for each **code** block assigned to a group, **modifying** the graph such
that arcs that previously pointed to the code block point instead to a
node representing the group; determining a difference between a...

11/6,K/13 (Item 3 from file: 349)
DIALOG(R)File 349:(c) 2006 WIPO/Univentio. All rts. reserv.

00344642

**SYSTEMS AND METHODS FOR SECURE TRANSACTION MANAGEMENT AND ELECTRONIC RIGHTS
PROTECTION**

**SYSTEMES ET PROCEDES DE GESTION SECURISEE DE TRANSACTIONS ET DE PROTECTION
ELECTRONIQUE DES DROITS**

Publication Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 207972

Publication Year: 1996

Fulltext Availability:

Detailed Description

Detailed Description

... may hit limitations of a single threaded
device in certain circumstances.

It is preferable when these limitations are unacceptable to
use a full "multi-threaded" **data structure** write capabilities. For
- 332

example, a type of "two-phase commit" processing of the type
used by database vendors may be used to allow **data structure**
sharing between processes. To implement this 'two-phase
commit' **process**, each swap **block** may contain page addresses for
additional memory blocks that will be used to store changed
information. A change page is a local copy of a piece of a data
element that has been written by an SPE process. The **changed**
page(s) references associated with a specific **data structure** are
stored locally to the swap block in the preferred embodiment.

For example, SPE 503 may support two (change pages) per
data structure. This limit...

11/6,K/14 (Item 4 from file: 349)

DIALOG(R)File 349:(c) 2006 WIPO/Univentio. All rts. reserv.

00234265 **Image available**

SYSTEM FOR DIVIDING PROCESSING TASKS INTO SIGNAL PROCESSOR AND
DECISION-MAKING MICROPROCESSOR INTERFACING
SYSTEME DE SEPARATION DES TACHES DE TRAITEMENT EN TACHES POUR INTERFACAGE
AVEC UN PROCESSEUR DE SIGNAUX ET UN MICROPROCESSEUR DE PRISE DE
DECISION

Publication Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 219172

Publication Year: 1993

Fulltext Availability:

Claims

Claim

... by a C compiler, the file must be in a different format than the
standard symbol file. To create this special version of the symbol **file**
, the symbol **translator** (SymTran) takes as input the symbol file
generated by the SPROCbuild utility and produces C header and code files
that create a **data structure** mirroring the symbol file and including
all necessary variable declarations. The symbol **translator** produces one
header **file** and one code file for each signal **processing** design.

E.5 Signal Processing Design Considerations

In order for a signal processing design created in the SPROCIab
development system to be usable in a...

11/6,K/15 (Item 5 from file: 349)
DIALOG(R) File 349:(c) 2006 WIPO/Univentio. All rts. reserv.

00149051

MULTIPROCESSING METHOD AND ARRANGEMENT
PROCEDE ET AGENCEMENT A MULTIPROCESSEUR

Publication Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 9571

Publication Year: 1988

Fulltext Availability:

Detailed Description

Detailed Description

... word, initial

stack pointer stack lower bound, and -stack upper bound),
the initialization is done by copying over the entire
contents of the 'original' **process** control **block** ,, to
simplify the **code** .

Up to now all **modifications** of private memory
have been performed on private memory 101 of master
processor 12 and must be replicated for the slave
processor's private memory. This replication is done by
copying a dpccram-t **data structure** , which contains all
per-processor data elements and which is now resident in
private memory 101 of master processor 12r to private
memory 101 of...

11/6,K/16 (Item 6 from file: 349)
DIALOG(R)File 349:(c) 2006 WIPO/Univentio. All rts. reserv.

00149050

**MULTIPROCESSING METHOD AND ARRANGEMENT
PROCEDE ET AGENCEMENT MULTIPROCESSEURS**

Publication Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 9315

Publication Year: 1988

Fulltext Availability:

Detailed Description

Detailed Description

... status word, initial

stack pointer, stack lower boundr and stack upper bound),
the initialization is done by copying over the entire
contents of the "original" **process** control **blockv** to
simplify the **code** .

Up to nowy all **modifications** of private memory
have been performed on private memory 101 of master
processor 12 and must be replicated for the slave
processor's private memory. This replication is done by
copying a dpccramt **data** **structurer** which contains all
per-processor data elements and which is now resident in
private memory 101 of master processor 12r to private
memory 101 of...

File 347:JAPIO Dec 1976-2005/Dec(Updated 060404)

(c) 2006 JPO & JAPIO

File 350:Derwent WPIX 1963-2006/UD,UM &UP=200638

(c) 2006 The Thomson Corp.

Set	Items	Description
S1	5779	(PORT? ? OR PORTAL OR PORTED OR PORTING) (5N) (SOFTWARE OR PROGRAM? ? OR APPLICATION? ? OR CODE? ? OR GAME? ? OR APPLET? ? OR THREAD? ? OR MULTITHREAD? ? OR MULTI()THREAD? ? OR FILE? ? OR MACRO? ? OR SCRIPT?)
S2	163	(PORT? ? OR PORTAL OR PORTED OR PORTING) (5N) (APP OR APPS OR BROWSER? OR WEBBROWSER? OR SUBROUTIN? OR SUBPROGRAM? OR OS OR OPERATING()SYSTEM? OR EXECUT?() (FILE? ? OR CODE? ? OR BYTE? - ?))
S3	5908	S1:S2
S4	2171123	(SOFTWARE OR PROGRAM? ? OR APPLICATION? ? OR CODE? ? OR GAME? ? OR APPLET? ? OR THREAD? ? OR MULTITHREAD? ? OR MULTI()THREAD? ? OR FILE? ? OR MACRO? ? OR SCRIPT?)
S5	58948	(APP OR APPS OR BROWSER? OR WEBBROWSER? OR SUBROUTIN? OR SUBPROGRAM? OR OS OR OPERATING()SYSTEM? OR EXECUT?() (FILE? ? OR CODE? ? OR BYTE? ?))
S6	130739	S4:S5(5N) (CONVERT??? OR ADJUST???? OR CHANG??? OR ADAPT? OR CONVERSION? OR ALTER??? OR MODIFY??? OR TRANSLAT? OR TRANSFORM? OR MODIFICATION? ?)
S7	11980	DATASTRUCTUR??? OR DATA()STRUCTUR???
S8	6126	PROCESS??? (2W)BLOCK? ?
S9	10	S7(20N)S8
S10	1	S3(30N)S8
S11	63	S6(30N)S8
S12	247	VIRTUALI?AT?
S13	0	S11(100N)S12
S14	624447	(METHOD? OR ACTION? ? OR COURSE? ? OR EVOLUTION OR FORMATION? ? OR FORM??? OR MANNER? ? OR MECHANISM? ? OR MODE? ? OR OPERAT???) (30N) (PLAN OR CHARACTERI? OR CHART??? OR DESCRI? OR LAY()OUT OR LAYOUT)
S15	1099604	(METHOD? OR ACTION? ? OR COURSE? ? OR EVOLUTION OR FORMATION? ? OR FORM??? OR MANNER? ? OR MECHANISM? ? OR MODE? ? OR OPERAT???) (30N) (PLOT? ? OR PLOTTING OR ARRANG? OR BLUEPRINT? ? OR CALCULAT? OR DESIGN?)
S16	784615	(METHOD? OR ACTION? ? OR COURSE? ? OR EVOLUTION OR FORMATION? ? OR FORM??? OR MANNER? ? OR MECHANISM? ? OR MODE? ? OR OPERAT???) (30N) (FORMULAT? OR FRAM??? OR MAP???? OR ORGANI?AT? - OR ORGANI???? OR OUTLIN???)
S17	1392454	(METHOD? OR ACTION? ? OR COURSE? ? OR EVOLUTION OR FORMATION? ? OR FORM??? OR MANNER? ? OR MECHANISM? ? OR MODE? ? OR OPERAT???) (30N) (REPRESENT? OR SCHEM??? OR CONSTRUCT??? OR UNIT? ? OR CONSTITUENT? ? OR DETAIL???)
S18	766505	(METHOD? OR ACTION? ? OR COURSE? ? OR EVOLUTION OR FORMATION? ? OR FORM??? OR MANNER? ? OR MECHANISM? ? OR MODE? ? OR OPERAT???) (30N) (MODULE? ? OR SECTION? ? OR SEGMENT? ?)
S19	220845	(PROCEDURE? ? OR PROCEEDING? ? OR PROGRESS??? OR PROGRESSION? ? OR ROUTINE? ? OR SUBROUTINE? ? OR RULE? ? OR STAGE? ? OR STEP? ? OR SYSTEM? ? OR TECHNIQUE? ?) (30N) (PLAN OR CHARACTERI? OR CHART??? OR DESCRI? OR LAY()OUT OR LAYOUT)
S20	351964	(PROCEDURE? ? OR PROCEEDING? ? OR PROGRESS??? OR PROGRESSION? ? OR ROUTINE? ? OR SUBROUTINE? ? OR RULE? ? OR STAGE? ? OR STEP? ? OR SYSTEM? ? OR TECHNIQUE? ?) (30N) (PLOT? ? OR PLOTTING OR ARRANG? OR BLUEPRINT? ? OR CALCULAT? OR DESIGN?)
S21	187335	(PROCEDURE? ? OR PROCEEDING? ? OR PROGRESS??? OR PROGRESSION? ? OR ROUTINE? ? OR SUBROUTINE? ? OR RULE? ? OR STAGE? ? OR STEP? ? OR SYSTEM? ? OR TECHNIQUE? ?) (30N) (FORMULAT? OR FRAM-

??? OR MAP???? OR ORGANI?AT? OR ORGANI???? OR OUTLIN???)
 S22 485536 (PROCEDURE? ? OR PROCEEDING? ? OR PROGRESS??? OR PROGRESSI-
 ON? ? OR ROUTINE? ? OR SUBROUTINE? ? OR RULE? ? OR STAGE? ? OR
 STEP? ? OR SYSTEM? ? OR TECHNIQUE? ?) (30N) (REPRESENT? OR SCH-
 EM??? OR CONSTRUCT??? OR UNIT? ? OR CONSTITUENT? ? OR DETAIL?-
 ??)
 S23 201452 (PROCEDURE? ? OR PROCEEDING? ? OR PROGRESS??? OR PROGRESSI-
 ON? ? OR ROUTINE? ? OR SUBROUTINE? ? OR RULE? ? OR STAGE? ? OR
 STEP? ? OR SYSTEM? ? OR TECHNIQUE? ?) (30N) (MODULE? ? OR SECT-
 ION? ? OR SEGMENT? ?)
 S24 4532758 S14:S23
 S25 3553394 S24 AND PY<=2002
 S26 0 S11(50N) (PORT? ? OR PORTAL OR PORTED OR PORTING)
 S27 0 S26 AND PY<=2002
 S28 67317 S24(50N) (PORT? ? OR PORTAL OR PORTED OR PORTING)
 S29 16182 S28(20N) (PORTING OR PORTED OR PORTS)
 S30 16119 S28(10N) (PORTING OR PORTED OR PORTS)
 S31 16096 S28(5N) (PORTING OR PORTED OR PORTS)
 S32 13039 S31 AND PY<=2002
 S33 2 S32(20N) S8

9/3,K/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2006 JPO & JAPIO. All rts. reserv.

05597830 **Image available**
GRAPHIC PRODUCTION DEVICE

PUB. NO.: 09-212630 [JP 9212630 A]
PUBLISHED: August 15, 1997 (19970815)
INVENTOR(s): UENO KOJI
SHIGEMI SATOSHI
APPLICANT(s): HONDA MOTOR CO LTD [000532] (A Japanese Company or
Corporation), JP (Japan)
APPL. NO.: 08-040281 [JP 9640281]
FILED: February 05, 1996 (19960205) .

ABSTRACT

PROBLEM TO BE SOLVED: To easily recognize the processing contents and the connection relation of every **processing block** based on the graphic data on a flowchart by producing a graphic by means of a composite graphic **data structure** where the **processing block** graphic data are combined with the character frame data describing the processing contents, etc., into a single graphic...

9/3,K/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2006 JPO & JAPIO. All rts. reserv.

03313433 **Image available**
ELECTRONIC APPARATUS

PUB. NO.: 02-288933 [JP 2288933 A]
PUBLISHED: November 28, 1990 (19901128)
INVENTOR(s): AMARI TAKASHI
APPLICANT(s): CANON INC [000100] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 01-043300 [JP 8943300]
FILED: February 27, 1989 (19890227)
JOURNAL: Section: P, Section No. 1166, Vol. 15, No. 63, Pg. 135,
February 14, 1991 (19910214)

ABSTRACT

PURPOSE: To protect data on a memory by certainly checking the output of a power supply device at the time of the data **processing** like **block transfer** which is interrupted to probably cause destruction of the **data structure** on the memory and inhibiting the data processing in case of abnormality of power supply...

9/3,K/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2006 The Thomson Corp. All rts. reserv.

017642057 **Image available**
WPI Acc No: 2006-153315/200616
XRPX Acc No: N06-132439

Query processing method, involves establishing query block information for inner query block if previously-generated query block information record exists in data structure, and determining cost for semantically equivalent query

Patent Assignee: ORACLE INT CORP (ORAC-N)

Inventor: AHMED R

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20060026115	A1	20060202	US 2004901272	A	20040727	200616 B

Priority Applications (No Type Date): US 2004901272 A 20040727

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 20060026115	A1	14	G06F-017/30	

Abstract (Basic):

... The method involves checking a **data structure** to determine whether a previously-generated query block information record corresponding to an already- **processed** inner query **block** exists in the structure. Query block information is established for the inner query block if the previously-generated record exists in the structure. A cost...

9/3,K/4 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2006 The Thomson Corp. All rts. reserv.

016022995 **Image available**
WPI Acc No: 2004-180846/200417
XRPX Acc No: N04-143776

**Encrypting/decrypting device encrypts or decrypts processing block
input data output by data structure analyzer, based on data
controller output cipher block chaining or cipher feedback mode selection
signal**

Patent Assignee: MATSUSHITA ELECTRIC IND CO LTD (MATU); FUKUOKA T
(FUKU-I); WADA T (WADA-I)

Inventor: FUKUOKA T; WADA T

Number of Countries: 031 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200415916	A1	20040219	WO 2003JP10186	A	20030808	200417 B
EP 1531578	A1	20050518	EP 2003784640	A	20030808	200533
			WO 2003JP10186	A	20030808	
KR 2005032588	A	20050407	KR 2005701976	A	20050203	200564
JP 2004527392	X	20051202	WO 2003JP10186	A	20030808	200580
			JP 2004527392	A	20030808	
US 20050286720	A1	20051229	WO 2003JP10186	A	20030808	200603
			US 2005523720	A	20050207	
CN 1675877	A	20050928	CN 2003819018	A	20030808	200610

Priority Applications (No Type Date): JP 2002231284 A 20020808

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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WO 200415916	A1	J	51	H04L-009/06	
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Designated States (National): CN JP KR US

Designated States (Regional): AT BE BG CH CY CZ DE DK EE ES FI FR GB GR
HU IE IT LU MC NL PT RO SE SI SK TR

EP 1531578	A1	E		H04L-009/06	Based on patent WO 200415916
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Designated States (Regional): AT BE BG CH CY CZ DE DK EE ES FI FR GB GR
HU IE IT LI LU MC NL PT RO SE SI SK TR

KR 2005032588	A			H04L-009/06	
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JP 2004527392	X		50	G09C-001/00	Based on patent WO 200415916
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US 20050286720	A1			H04K-001/00	
----------------	----	--	--	-------------	--

CN 1675877	A			H04L-009/06	
------------	---	--	--	-------------	--

**Encrypting/decrypting device encrypts or decrypts processing block
input data output by data structure analyzer, based on data
controller output cipher block chaining or cipher feedback mode selection
signal**

Abstract (Basic):

... A data structure analyzer (2) receives encrypted data or
data to be encrypted and outputs as processing block input data,
control data. A data controller (6) outputs cipher block chaining (CBC)
or cipher feedback (CFB) mode selection signals based on the received
control...

9/3,K/5 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2006 The Thomson Corp. All rts. reserv.

015771744 **Image available**
WPI Acc No: 2003-833946/200377
XRPX Acc No: N03-666641

**Digital two way communication control device analyses data structure of
traffic encryption key processing data obtained from format converted
downstream data for data decoding**

Patent Assignee: MATSUSHITA ELECTRIC IND CO LTD (MATU); MATSUSHITA DENKI
SANGYO KK (MATU); FUKUOKA T (FUKU-I); WADA T (WADA-I)

Inventor: FUKUOKA T; WADA T

Number of Countries: 031 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200388557	A1	20031023	WO 2003JP4864	A	20030416	200377 B
JP 2003309547	A	20031031	JP 2002114076	A	20020417	200380
EP 1496640	A1	20050112	EP 2003717606	A	20030416	200504
			WO 2003JP4864	A	20030416	
KR 2004090968	A	20041027	KR 2004710661	A	20040708	200516
US 20050147251	A1	20050707	WO 2003JP4864	A	20030416	200547
			US 2004511135	A	20041014	
CN 1633775	A	20050629	CN 2003803955	A	20030416	200574

Priority Applications (No Type Date): JP 2002114076 A 20020417

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
WO 200388557	A1	J 50	H04L-009/00	
			Designated States (National):	CN KR US
			Designated States (Regional):	AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT RO SE SI SK TR
JP 2003309547	A	19	H04L-009/08	
EP 1496640	A1	E	H04L-009/00	Based on patent WO 200388557
			Designated States (Regional):	AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LU MC NL PT RO SE SI SK TR
KR 2004090968	A		H04L-009/00	
US 20050147251	A1		G06F-012/14	
CN 1633775	A		H04L-009/00	

Abstract (Basic):

... converts the format of received downstream data (STRM) on
receiving the format converted data, a CPU (12) executes media access
control (MAC) function while a **processing block** (13) analyzes the
data structure of a traffic encryption key (TEK) processing data
obtained from the interface block (DIF). According to the analysis
result, the data is decoded.

9/3,K/6 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2006 The Thomson Corp. All rts. reserv.

014884947 **Image available**
WPI Acc No: 2002-705653/200276
XRPX Acc No: N02-556244

**Processing fault handling method in computer system, involves repeating
detecting faults and initiating execution of instructions according to
restart sequences which restarts without and with lag time**

Patent Assignee: CISCO TECHNOLOGY INC (CISC-N)

Inventor: SINGH D; WACLAWSKY J G

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6453430	B1	20020917	US 99305947	A	19990506	200276 B

Priority Applications (No Type Date): US 99305947 A 19990506

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6453430	B1	20	G06F-011/00		

Abstract (Basic):

... 3) **Process control block data structure ; and...**

9/3,K/7 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2006 The Thomson Corp. All rts. reserv.

014011810 **Image available**
WPI Acc No: 2001-496024/200154
XRPX Acc No: N01-367536

Computer readable storage medium for locating software object in distributed computer system, has functional block conveying a persistent name to create entry in data structure if name is not found in other data structure

Patent Assignee: NORTEL NETWORKS LTD (NELE)

Inventor: QUIRT A R

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6269378	B1	20010731	US 98219313	A	19981223	200154 B

Priority Applications (No Type Date): US 98219313 A 19981223

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 6269378	B1	17	G06F-017/30	

Abstract (Basic):

... An interface functional block permits a name service to receive locate request messages. The **data structures** store data elements mapping persistent names of software objects and data indicating unresolved locate request messages respectively. A **processing functional block** responsive to locate request message conveys certain persistent name to create an entry in a **data structure** associated with the persistent name if the name is not found in the other data structure.

9/3,K/8 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2006 The Thomson Corp. All rts. reserv.

011915921 **Image available**
WPI Acc No: 1998-332831/199829
XRPX Acc No: N98-259849

**Distributed computer system with distributed shared memory connected to
network - executes load instruction if data loaded from shared data
structure are different from predetermined flag value**

Patent Assignee: DIGITAL EQUIP CORP (DIGI)

Inventor: SCALES D J

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5761729	A	19980602	US 96672221	A	19960717	199829 B

Priority Applications (No Type Date): US 96672221 A 19960717

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5761729	A	24	G06F-012/00	

...Abstract (Basic): of the memories is designated as virtual shared
address, for storing shared data. A portion of the virtual shared
address is allocated to store shared **data structure** as one or more
blocks accessed by the programs executed in any one of the **processors**
. Each **block** includes integer number of lines where each line
includes predetermined number of bytes...

9/3,K/9 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2006 The Thomson Corp. All rts. reserv.

010123166 **Image available**
WPI Acc No: 1995-024417/199504
XRPX Acc No: N95-018938

**Emulation system for multi-tasking pipelines in single tasking
environment - uses pipeline of initialised instantiations of one or more
tasks when host application needs data processed from data source**

Patent Assignee: XEROX CORP (XERO)
Inventor: VENABLE D L; VENABLE D A
Number of Countries: 006 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 629945	A2	19941221	EP 94304303	A	19940614	199504 B
CA 2121154	A	19941216	CA 2121154	A	19940413	199511
US 5396616	A	19950307	US 9376679	A	19930615	199515
EP 629945	A3	19950524	EP 94304303	A	19940614	199546
EP 629945	B1	19980225	EP 94304303	A	19940614	199812
DE 69408601	E	19980402	DE 94608601	A	19940614	199819
			EP 94304303	A	19940614	
CA 2121154	C	19990309	CA 2121154	A	19940413	199928
JP 3617852	B2	20050209	JP 94125268	A	19940607	200511

Priority Applications (No Type Date): US 9376679 A 19930615

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 629945	A2	E	26	G06F-009/38	
Designated States (Regional): DE FR GB					
CA 2121154	A			G06F-009/38	
US 5396616	A		24	G06F-009/455	
EP 629945	A3			G06F-009/38	
EP 629945	B1	E	33	G06F-009/46	
Designated States (Regional): DE FR GB					
DE 69408601	E			G06F-009/46	Based on patent EP 629945
CA 2121154	C			G06F-009/38	
JP 3617852	B2		20	G06F-009/46	Previous Publ. patent JP 7105021

...Abstract (Basic): of predefined data structures which can be linked
between host application and data source to create stream-oriented data
processing structure emulating UNIX-like pipeline **data structure** .
Provides efficient method for **processing data blocks** .

...Abstract (Equivalent): of predefined data structures which can be linked
between host application and data source to create stream-oriented data
processing structure emulating UNIX-like pipeline **data structure** .
Provides efficient method for **processing data blocks** .

9/3,K/10 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2006 The Thomson Corp. All rts. reserv.

008743359 **Image available**
WPI Acc No: 1991-247375/199134
XRPX Acc No: N91-188621

Peripheral controlling multi-tasking system - combines access to two data structures to provide process access to peripheral device

Patent Assignee: IBM CORP (IBM)
Inventor: FLURRY G A; HENSON L W
Number of Countries: 004 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 442717	A	19910821	EP 91301154	A	19910213	199134 B
EP 442717	A3	19930127	EP 91301154	A	19910213	199347

Priority Applications (No Type Date): US 90480186 A 19900213

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
EP 442717	A			

Designated States (Regional): DE FR GB IT

...Abstract (Basic): The data processing system has a peripheral device controller with a device data store block for providing **data structures** having data store block for providing **data structures** having data representing characteristics of the peripheral device. A **process** data storage **block** provides second **data structures** having data representing characteristics of each processe. Data from both the **data structures** is combined to permit access to the peripheral device by any given one of the processes...

10/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2006 The Thomson Corp. All rts. reserv.

016050824 **Image available**
WPI Acc No: 2004-208675/200420
Related WPI Acc No: 2000-324613
XRPX Acc No: N04-165741

Processing apparatus used for e.g. resist application in semiconductor wafer, has delivery port which delivers to-be processed object between main conveyance lines and each processing blocks

Patent Assignee: TOKYO ELECTRON LTD (TKEL)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2004056122	A	20040219	JP 98264165	A	19980918	200420 B
			JP 2003167883	A	20030612	

Priority Applications (No Type Date): JP 98264165 A 19980918; JP 2003167883 A 20030612

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2004056122	A	11	H01L-021/027	Div ex application JP 98264165

Processing apparatus used for e.g. resist application in semiconductor wafer, has delivery port which delivers to-be processed object between

main conveyance lines and each processing blocks

33/3,K/1 (Item 1 from file: 347)

DIALOG(R)File 347:JAPIO

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06220076 **Image available**

PARALLEL SYSTEM FOR EXECUTING ARRAY PROCESSING IN SHORT WAIT TIME BY USING
FAST FOURIER TRANSFORMATION

PUB. NO.: 11-161637 [JP 11161637 A]

PUBLISHED: June 18, 1999 (19990618)

INVENTOR(s): JU CHWEN-JYE
SIDMAN STEVEN B

APPLICANT(s): SHARP CORP
SHARP MICRO ELECTRON TECHNOL INC

APPL. NO.: 10-255661 [JP 98255661]

FILED: September 09, 1998 (19980909)

PRIORITY: 58592 [US 58592], US (United States of America), September
12, 1997 (19970912)

ABSTRACT

... connection and design by minimizing the wait time of fast Fourier transformation.

SOLUTION: Between memory units A(q) and B(q) which are addressable memory **units** provided at **ports** A and B of execution **units**, data are moved in a selected sequence through the respective execution **units** P(q) to process data in Y processing **stages**. A data router distributes N data points between the addressable memory **units** and respective memory **units** A, which receive N/Z data points respectively; and the respective execution **units** **process blocks** including the N/Z data points in Y processing **stages** and the processes are performed in parallel. Consequently, the N data points are processed in Z parallel streams through Z execution **units**.

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33/3,K/2 (Item 2 from file: 347)

DIALOG(R)File 347:JAPIO

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04708387 **Image available**

VIDEO SIGNAL PROCESSOR

PUB. NO.: 07-028987 [JP 7028987 A]

PUBLISHED: January 31, 1995 (19950131)

INVENTOR(s): NAKAI SEIJI
KUBOTA TADASHI
NISHIO TOSHIAKI
SUZUKI HIDEKAZU
SEDO KOJI

APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company
or Corporation), JP (Japan)

APPL. NO.: 05-174067 [JP 93174067]

FILED: July 14, 1993 (19930714)

ABSTRACT

...CONSTITUTION: A dual **port** DRAM 120 provided with a new function is used for storing the **frame** data, the processors 110 and 111 for a movement compensation processing requiring random access are connected to a random access **port**, the processor for the DCT arithmetic **operation**, the processors 112 and 113 for a movement detection **processing** requiring **block** access are connected to plural serial access **ports** capable of access in the lateral/longitudinal/zigzag directions of the frame data and the video encoding processing is performed.

File 8: Ei Compendex(R) 1970-2006/Jun W2
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File 35: Dissertation Abs Online 1861-2006/May
(c) 2006 ProQuest Info&Learning
File 65: Inside Conferences 1993-2006/Jun 20
(c) 2006 BLDSC all rts. reserv.
File 2: INSPEC 1898-2006/Jun W2
(c) 2006 Institution of Electrical Engineers
File 94: JICST-EPlus 1985-2006/Mar W3
(c) 2006 Japan Science and Tech Corp(JST)
File 483: Newspaper Abs Daily 1986-2006/Jun 19
(c) 2006 ProQuest Info&Learning
File 6: NTIS 1964-2006/Jun W2
(c) 2006 NTIS, Intl Cpyrghrt All Rights Res
File 144: Pascal 1973-2006/May W4
(c) 2006 INIST/CNRS
File 434: SciSearch(R) Cited Ref Sci 1974-1989/Dec
(c) 1998 Inst for Sci Info
File 34: SciSearch(R) Cited Ref Sci 1990-2006/Jun W2
(c) 2006 Inst for Sci Info
File 99: Wilson Appl. Sci & Tech Abs 1983-2006/May
(c) 2006 The HW Wilson Co.
File 583: Gale Group Globalbase(TM) 1986-2002/Dec 13
(c) 2002 The Gale Group
File 266: FEDRIP 2005/Dec
Comp & dist by NTIS, Intl Copyright All Rights Res
File 95: TEME-Technology & Management 1989-2006/Jun W3
(c) 2006 FIZ TECHNIK
File 62: SPIN(R) 1975-2006/Mar W4
(c) 2006 American Institute of Physics
File 239: Mathsci 1940-2006/Jul
(c) 2006 American Mathematical Society

Set	Items	Description
S1	17234	(SOFTWARE OR PROGRAM? ? OR APPLICATION? ? OR CODE? ? OR GAME? ? OR APPLET? ? OR THREAD? ? OR MULTITHREAD? ? OR MULTI()T-HREAD? ? OR FILE? ? OR MACRO? ? OR SCRIPT?) (5N)PORT???
S2	1080	(APP OR APPS OR BROWSER? OR WEBBROWSER? OR SUBROUTIN? OR SUBPROGRAM? OR OS OR OPERATING()SYSTEM? OR EXECUT?() (FILE? ? OR CODE? ? OR BYTE? ?)) (5N)PORT???
S3	18089	S1:S2
S4	11366824	(SOFTWARE OR PROGRAM? ? OR APPLICATION? ? OR CODE? ? OR GAME? ? OR APPLET? ? OR THREAD? ? OR MULTITHREAD? ? OR MULTI()T-HREAD? ? OR FILE? ? OR MACRO? ? OR SCRIPT?)
S5	368553	(APP OR APPS OR BROWSER? OR WEBBROWSER? OR SUBROUTIN? OR SUBPROGRAM? OR OS OR OPERATING()SYSTEM? OR EXECUT?() (FILE? ? OR CODE? ? OR BYTE? ?))
S6	344620	S4:S5(5N) (CONVERT??? OR ADJUST???? OR CHANG??? OR ADAPT? OR CONVERSION? OR ALTER??? OR MODIFY??? OR TRANSLAT? OR TRANSFORM? OR MODIFICATION? ?)
S7	113486	DATASTRUCTUR??? OR DATA()STRUCTUR???
S8	4875	PROCESS??? (2W)BLOCK? ?
S9	7	S7(20N)S8
S10	7	S3(30N)S8
S11	225	S6(30N)S8
S12	14	S9 OR S10
S13	3	S11 AND PORT???
S14	15	S12 OR S13
S15	13	RD (unique items)
S16	11	S15 AND PY<=2002

16/7/1 (Item 1 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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08514057 E.I. No: EIP01035582563

Title: Memory efficient software synthesis with mixed coding style from dataflow graphs

Author: Sung, Wonyong; Ha, Soonhoi
Corporate Source: Seoul Natl Univ, Seoul, S Korea
Conference Title: 11th International Symposium on System-Level Synthesis and Design (ISS'98)
Conference Location: Hsinchu, Taiwan Conference Date: 20981202-20981204
Sponsor: IEEE CS Technical Committee on Design Automation; ACM SIGDA
E.I. Conference No.: 57950
Source: IEEE Transactions on Very Large Scale Integration (VLSI) Systems v 8 n 5 Oct 2000. p 522-526
Publication Year: 2000
CODEN: IEVSE9 ISSN: 1063-8210
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical)
Journal Announcement: 0105W1

Abstract: This paper presents a set of techniques to reduce the code and data sizes for software synthesis from graphical digital signal-processing programs based on the synchronous dataflow model. By sharing the kernel code among multiple instances of a block with a shared function, we can further reduce the code size below the previous results based on inline coding style. A systematic approach also is devised to give up the single appearance schedule for reducing the data buffer requirement. The proposed techniques have been evaluated with two real-life examples to prove their significance. (Author abstract) 7 Refs.

16/7/2 (Item 2 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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04533870 E.I. No: EIP96103369601

Title: Telekom's MAGENTA algorithm for en-/decryption in the gigabit/sec range

Author: Huber, Klaus; Wolter, Stefan
Corporate Source: Deutsche Telekom, Darmstadt, Ger
Conference Title: Proceedings of the 1996 IEEE International Conference on Acoustics, Speech, and Signal Processing, ICASSP. Part 6 (of 6)
Conference Location: Atlanta, GA, USA Conference Date: 19960507-19960510
Sponsor: IEEE
E.I. Conference No.: 45447
Source: ICASSP, IEEE International Conference on Acoustics, Speech and Signal Processing - Proceedings v 6 1996. IEEE, Piscataway, NJ, USA, 96CB35903. p 3233-3235
Publication Year: 1996
CODEN: IPRODJ ISSN: 0736-7791
Language: English
Document Type: CA; (Conference Article) Treatment: G; (General Review); T; (Theoretical)

Journal Announcement: 9612W3

Abstract: The Deutsche Telekom is currently considering the development of an en-/decryption module for wide-spread (internal) usage. For this purpose a block-cipher algorithm has been developed by the Deutsche Telekom. The algorithm named MAGENTA which stands for Multifunctional Algorithm for General-purpose Encryption and Network Telecommunication

Applications, is based on the shuffle signal-flow structure combined with non-linear operations. The module is planned to operate in the Gigabit/sec range for fast networks. For such high data rates there is a need of block-cipher hardware. (Author abstract) 4 Refs.

16/7/3 (Item 3 from file: 8)
DIALOG(R) File 8: Ei Compendex(R)
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02077713 E.I. Monthly No: EIM8603-015077

Title: FUNCTIONAL MAPPING FOR MICROPROCESSOR SYSTEM SIMULATION.

Author: Marshall, W. K.; Zobrist, G. W.; Bach, W.; Richardson, A.

Corporate Source: Univ of Missouri at Rolla, Graduate Engineering Cent, St. Louis, MO, USA

Conference Title: 1985 IEEE Microprocessor Forum: Design Productivity Through Engineering Workstations.

Conference Location: Atlantic City, NJ, USA Conference Date: 19850402

Sponsor: IEEE Computer Soc, Los Alamitos, CA, USA.; IEEE, New York, NY, USA.

E.I. Conference No.: 07657

Source: Publ by IEEE, New York, NY, USA Available from IEEE Service Cent (Cat n 85CH2151-9), Piscataway, NJ, USA p 15-19

Publication Year: 1985

ISBN: 0-8186-0616-9

Language: English

Document Type: PA; (Conference Paper)

Journal Announcement: 8603

Abstract: The object code portion of a microprocessor must be modeled in order to functionally simulate a microprocessor-based electronic system. The automated technique presented here for creating functionally equivalent high-level **programs** for the executable **portion** of the **software** represents one step towards the total automation of the simulation model building **process**. The **block** primitives provide a convenient way to simulate sections of the microcode rather than individual statements. The instruction timing preserved for each block can be incorporated into the simulation in order to maintain timing resolution with respect to other simulation models. The table-lookup-driven translation scheme makes switching possible between a variety of simulation languages with minimal changes to the translator software. 6 refs.

16/7/4 (Item 4 from file: 8)
DIALOG(R) File 8: Ei Compendex(R)
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02041766 E.I. Monthly No: EI8611107490 E.I. Yearly No: EI86030685

Title: HIGH-SPEED MULTI-PROGRAMMING DATA STRUCTURE.

Author: Anon

Source: IBM Technical Disclosure Bulletin v 29 n 2 Jul 1986 p 947

Publication Year: 1986

CODEN: IBMTAA ISSN: 0018-8689

Language: ENGLISH

Document Type: JA; (Journal Article) Treatment: A; (Applications)

Journal Announcement: 8611

Abstract: A method is described to provide a fast context switching function in a hardware environment where there is a large amount of context data to be kept track of. When a Resource Manager of a multi-processing system is designed to support a real time environment for high speed I/O devices, it must be able to switch rapidly between various programs, and process frequent hardware interrupts. Generally, there is a large amount of

data associated with each program, or process, which must be saved when the process is interrupted and restored when the process is resumed. In accordance with the new method, to avoid unnecessary copying of data, the RM uses the process control block itself as the interrupt save area.

16/7/5 (Item 1 from file: 35)

DIALOG(R)File 35:Dissertation Abs Online
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01239466 ORDER NO: AAD92-22169

FAULT TOLERANT CHEMICAL REACTOR CONTROL

Author: BASILA, MICHAEL ROBERT, JR.

Degree: PH.D.

Year: 1991

Corporate Source/Institution: ILLINOIS INSTITUTE OF TECHNOLOGY (0091)

Source: VOLUME 53/05-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 2430. 332 PAGES

A supervisory Model-Object Based Expert Control System (MOBECS) has been developed to provide fault tolerant control of a chemical reactor. This supervisory process control expert system is capable of initializing the control system based upon the current operating conditions and monitoring the process and control system for faults or deteriorating performance. If a fault is detected, MOBECS can formulate and implement corrective actions ranging from automatic controller tuning through complete restructuring of the process control algorithm. If a primary sensor fails, the expert system can replace the missing measurement with a state estimator.

The architecture of the expert system is based upon a hybrid paradigm that uses a class-object structure to represent the process and control system with a rule based inference mechanism. The process control system uses a similar architecture based upon **process control function blocks**. This commonality of **data structures** gives MOBECS the ability to modify every facet of the control system in real time. An expert system design formalism, based upon the Entity-Relationship relational data base model was used to develop the expert system. MOBECS has been generalized to any type of process control system or unit operation. All of the process specific knowledge is confined to the objects in the knowledge base and the procedures called by the rules and metaslot methods. The expert system design was validated by applying it to a tubular, fixed bed, autothermal reactor in which carbon monoxide is oxidized to carbon dioxide over a platinum catalyst. MOBECS successfully tailored the Internal Model Control algorithms, used to control the reactor, in response to changes in the operating conditions and faults in the process control system.

16/7/6 (Item 2 from file: 35)

DIALOG(R)File 35:Dissertation Abs Online
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01154487 ORDER NO: NOT AVAILABLE FROM UNIVERSITY MICROFILMS INT'L.

CONTRIBUTIONS TO ARCHITECTURAL DESIGN IN DIGITAL SIGNAL PROCESSING

Author: LOFFLER, CHRISTOPH D.

Degree: DR.SC.TECH

Year: 1990

Corporate Source/Institution: EIDGENOSSISCHE TECHNISCHE HOCHSCHULE
ZURICH (SWITZERLAND) (0663)

Source: VOLUME 52/02-C OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 286. 276 PAGES

Publisher: HARTUNG-GORRE VERLAG, SAENTISBLICK 26, D-7750 KONSTANZ,

GERMANY

In this thesis, we present concepts and methods for high-level systems design in digital signal processing and the implementation of these concepts into a set of design tools.

Architectural design comprises the detailed steps necessary to implement an algorithm onto a signal processing architecture. The algorithm may exist only on an abstract or even "fuzzy" level, and the hardware-architecture may be defined only in very coarse terms. Typical target-architectures include parallel signal processors and VLSI chips.

Focusing on the integration of the necessary design tasks into one CAD package, we have achieved a design-system that allows work on different and mixed abstraction levels, and supports smooth transitions between these levels of hierarchy. An open, interactive system concept is aimed at assisting the designer rather than fully automating the design process.

A hierarchical, **block**-diagram-based **data structure** permits the expansion of both blocks and connections during top-down design, and allows a system to be modeled on user-defined hierarchical levels.

A compiled mixed-level simulator with user-programmed functional models can automatically be generated from the design-data description by a simulator-generator program. The simulation of different parts of a system is possible simultaneously on multiple abstraction levels. High-level data types may also be used directly in the simulation.

Contrary to current practice in algorithm-architecture mapping, we propose the systematic adaptation of both architecture and algorithm during the mapping process. The capability of hierarchical mapping, with iterative steps of scheduling and resource allocation on different abstraction levels significantly reduces the computation cost by splitting the tasks into small subtasks. It further helps the designers to influence the mapping process result according to the specific needs of their applications.

In addition to the CAD design tool for algorithm-architecture mapping, two extensions to static scheduling are presented and that permit efficient schedules to be implemented for if-statements and loop structures.

16/7/7 (Item 1 from file: 2)

DIALOG(R)File 2:INSPEC

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05539704 INSPEC Abstract Number: C9401-6150J-024

Title: Modifying OpenVMS process statuses

Author(s): Hunt, J.W.

Journal: Digital Systems Journal vol.15, no.4 p.25-7

Publication Date: July-Aug. 1993 Country of Publication: USA

CODEN: DSJOEE ISSN: 8750-9628

Language: English Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: If you have ever had a critical job accidentally killed, you may have wondered if there is a way to create an undeletable process. Although unsupported by Digital, a technique does exist. Every process on OpenVMS has associated with it a **data structure** known as a **process control block** (PCB). The PCB describes in great detail a good deal about the attributes of a process. A very important piece of information is PCB\$L-STS, which is the name implies, holds the process' status. By modifying this status field, one can make the process immune to deletion commands regardless of the callers' privileges. The author explains how to do this. (0 Refs)

Subfile: C

16/7/8 (Item 2 from file: 2)

DIALOG(R)File 2:INSPEC

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04560741 INSPEC Abstract Number: B90014148, C90013158

Title: Custom DSP chip extends instrument capabilities

Author(s): Kareen, A.

Author Affiliation: Tektronix, Beaverton, UK

Journal: Electronic Product Design vol.10, no.9 p.41-4, 47

Publication Date: Oct. 1989 Country of Publication: UK

CODEN: EPDEDB ISSN: 0263-1474

Language: English Document Type: Journal Paper (JP)

Treatment: Practical (P); Product Review (R)

Abstract: The test and measurement industry has already embraced DSP for new product concepts as well as for enhancing the capabilities of their existing product offering. A block diagram of a typical DSP based system is shown. The TriStar single-chip programmable digital signal processor uses a Harvard architecture, prefetched instructions, wide instruction word, two external data memories, and extensive parallelism to provide high performance and throughput in waveform processing. Although its architecture has been optimised for test instruments, the TriStar is capable of performing general digital signal **processing** tasks. The **block** diagram of the processor is shown. The chip includes a 16*32 bit three-**port** data register **file**, four 16*20 bit address register files, and a 16*20 bit instruction address stack. These elements are organised to form three major units: an arithmetic unit (AU), an address computation unit (ACU), and an instruction fetch unit (IFU), which all operate in parallel. The TriStar is a single cycle machine with all instructions executed in 150 nsec cycle time. The two Data memories and the instruction memory are separated to allow for simultaneous fetching of instructions and accessing of data. Communications between the units is via status flags and a register Bus. The AU internal data path is 32 bits wide allowing execution of many double precision (32 bit) operations. (0 Refs)

Subfile: B C

16/7/9 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

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02319529 INSPEC Abstract Number: C79009900

Title: Closing the software gap for interactive mini/microcomputation: direct execution of microprogrammed block-diagram primitives

Author(s): Korn, G.A.

Author Affiliation: Univ. of Arizona, Tucson, AZ, USA

Conference Title: Proceedings of COMPSAC 78 Computer Software and Applications Conference p.93-103

Publisher: IEEE, New York, NY, USA

Publication Date: 1978 Country of Publication: USA xiv+832 pp.

Conference Sponsor: IEEE

Conference Date: 13-16 Nov. 1978 Conference Location: Chicago, IL, USA

Language: English Document Type: Conference Paper (PA)

Treatment: General, Review (G)

Abstract: Block-diagram programs, for instrumentation, control, and simulation systems are especially easy to translate, since no explicit precedence analysis is needed. Block-diagram primitives range from simple adders to complete real-time controllers. They are pure-procedure, reentrant microprograms or threaded code in read-only memory, which may be pre-programmed and plugged in for special applications. In addition to hand 'assembly' and optimizing compilation of the block-diagram programs, the author exhibits the direct-executive MICRODARE II system, which embeds block-diagram 'assembly' in an advanced BASIC dialect serving for

interactive editing, job control, and file manipulation. Execution speeds of the systems permit LSI 11 microcomputers and PDP 11 minis to match and exceed those of a CDC 6400; a number of examples are shown. The report continues with a discussion of future multi-task, multiprocessor real-time BASIC systems incorporating MICRODARE. The author finally describes a new two-processor system consisting of an LSI-11 running MICRODARE **software** joined by a two- **port** memory to an ultra-fast bit-sliced 2903/2910 **processor** executing **block** -diagram microprograms. (13 Refs)

Subfile: C

16/7/10 (Item 1 from file: 6)

DIALOG(R)File 6:NTIS

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0687226 NTIS Accession Number: FE-2275-4/XAB

Systems Studies of Coal Conversion Processes Using a Reference Simulator. Quarterly Report, April 1, 1977--June 30, 1977

Reklaitis, G. V. ; Woods, J. M. ; Kayihan, F. ; Sood, M.

Purdue Univ., Lafayette, Ind.

Corp. Source Codes: 5347000

Sponsor: Department of Energy.

Jul 77 41p

Journal Announcement: GRAI7812; NSA0300

Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.

NTIS Prices: PC A03/MF A01

Contract No.: EX-76-C-01-2275

Preliminary user's manuals were prepared for the physical properties code package and for the **process block** material balancing code. These **codes** together with a major **portion** of the process equipment calculation system were released to ORNL, Lehigh University, and ERDA-Aberdeen. Significant process has been made in the pyrolysis section model and on the process equipment calculation system. Manuals for these codes are under preparation. The equipment calculation system has been linked with the properties package and expansion of the module library is proceeding. Development work has continued on the equipment costing system and the hydrotreating models. The cost data files have been implemented on the computer and work is in progress on the file manipulation and costing subroutines. Literature review is complete on the hydrotreating section and semi-empirical model equations have been assembled and fitted to available data. Further flowsheet modelling will be suspended until a base case flowsheet is developed. (ERA citation 03:013635)

16/7/11 (Item 1 from file: 144)

DIALOG(R)File 144:Pascal

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14580194 PASCAL No.: 00-0247543

Security analysis of block cipher BEAR

ZHU H; QU H; RAN L; WANG Y

Zhejiang Univ, Hangzhou, China

Journal: Chinese Journal of Electronics, 2000 , 9 (1) 29-32

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Pseudo-randomness and differential aspect of the unbalanced Feistel block cipher BEAR are mainly concerned in this paper. We have shown that two facts of block cipher BEAR. The order of pseudo-randomness of BEAR is $O(2t/2+2s/2)$, which implies that BEAR can resist $O(2t/2+2s/2)$ order plain-text attack. And the other fact is that if hash function can resist differential attack then so does the block cipher BEAR.